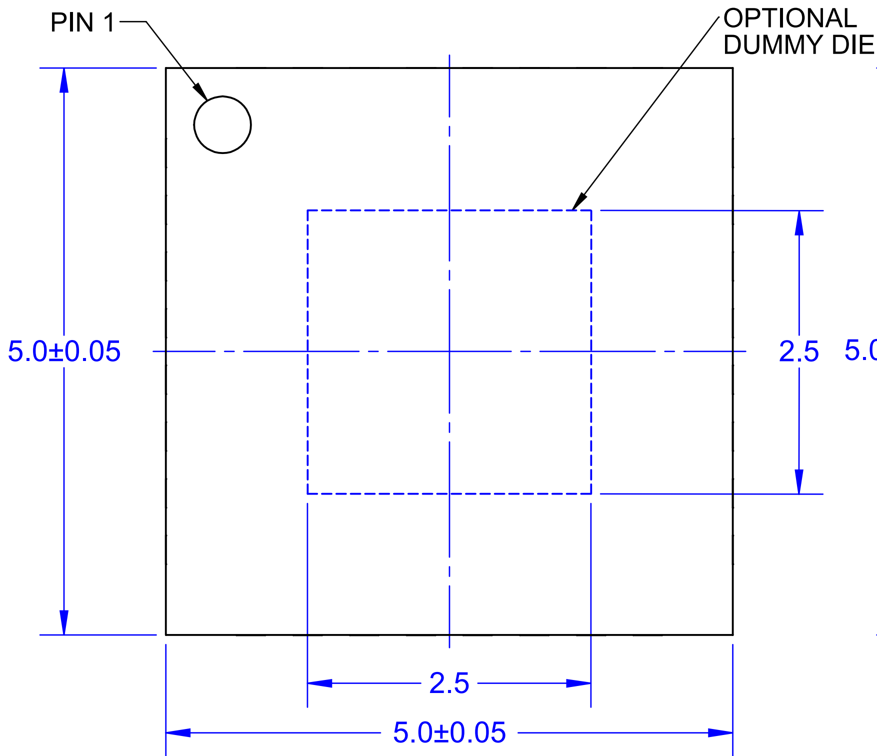
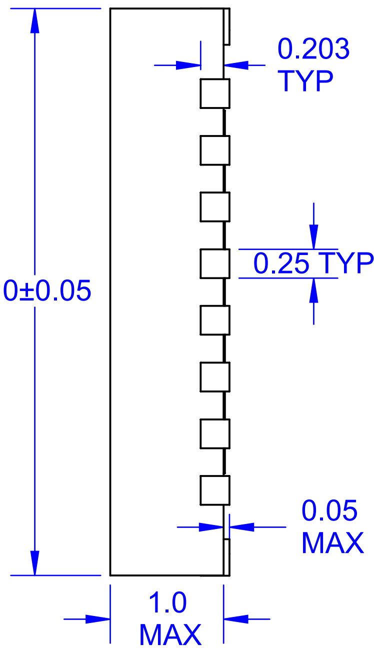
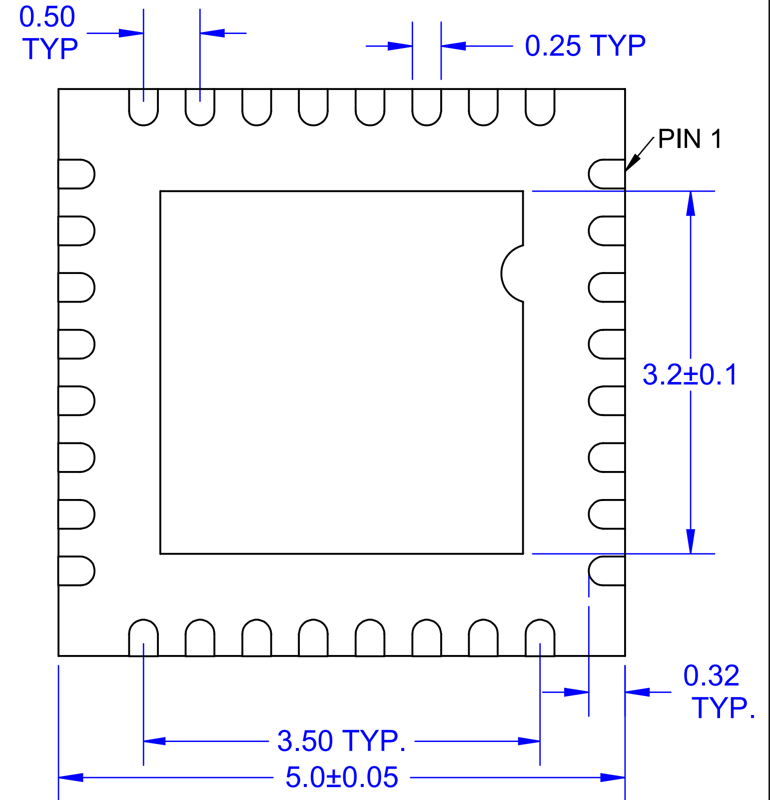
TOP VIEW



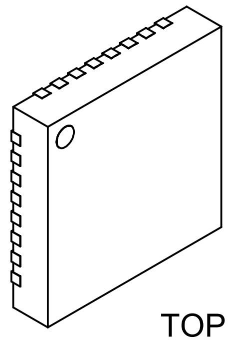
SIDE VIEW

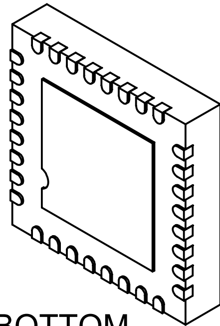


BOTTOM VIEW



MODEL



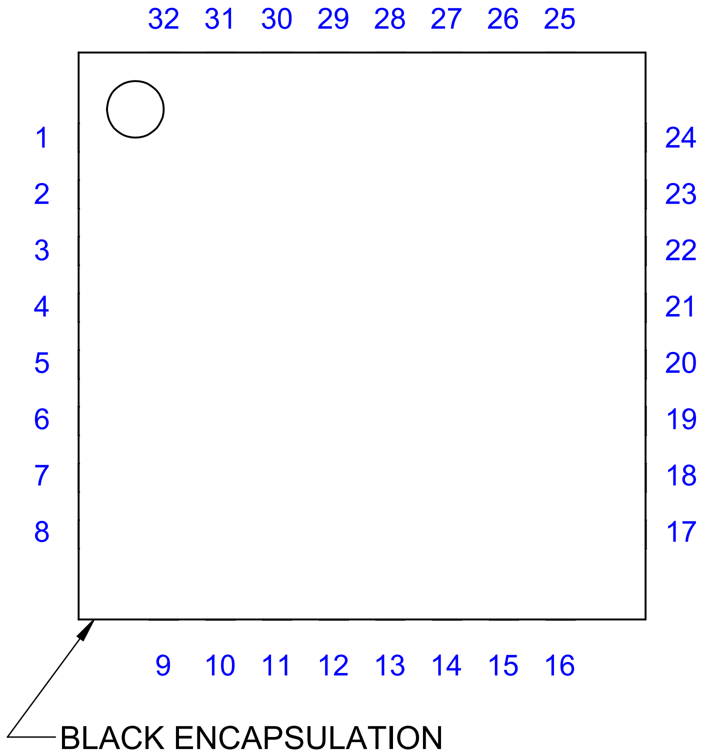


Notes: (Unless Otherwise Specified).
1) BODY: PLASTIC, SEMICONDUCTOR GRADE.
2) LEAD FRAME: COPPER, C-194 F/H.
3) PLATING Ni 2.5~7.6μm Au 1.0~2.0μm.
4) FRAME THICKNESS: 0.203mm.
5) DIE PAD: 3.2 x 3.2mm.
6) JEDEC OUTLINE: MO-220.
7) DIMENSIONS IN mm.

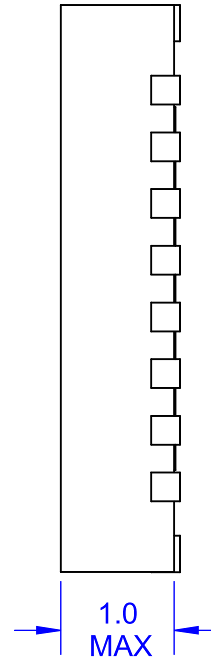
APPROVALS		DATE	TopLine®			
DRAWN	T.Au	9/18/2021				
ENG	M. Hart	9/18/2021	TITLE	32-LEAD 5mm P=0.5mm QFN PACKAGE		
MFG						
QA			SCALE 15:1	SIZE A	DRAWING NO. 453238	REV A
CUST						
REVISED			DO NOT SCALE DRAWING		SHEET 1 OF 5	

DAISY CHAIN PATTERN

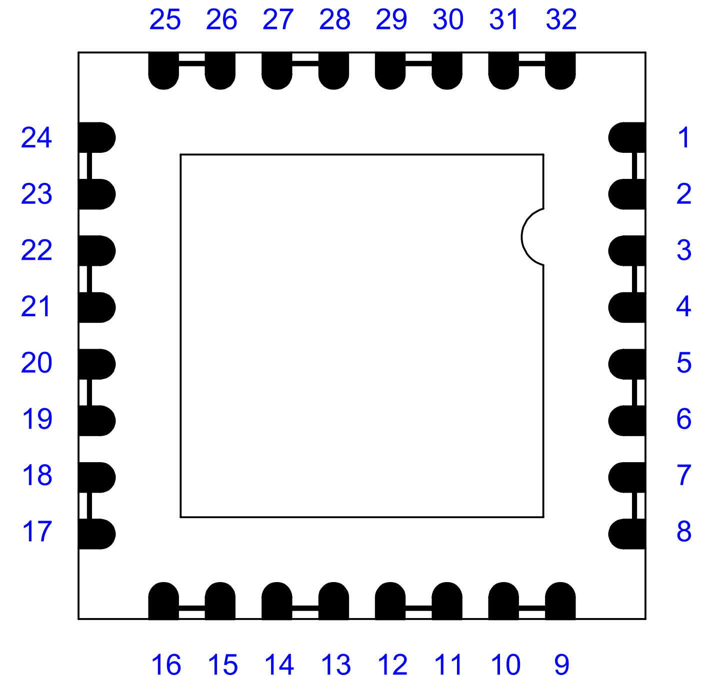
TOP VIEW



SIDE VIEW

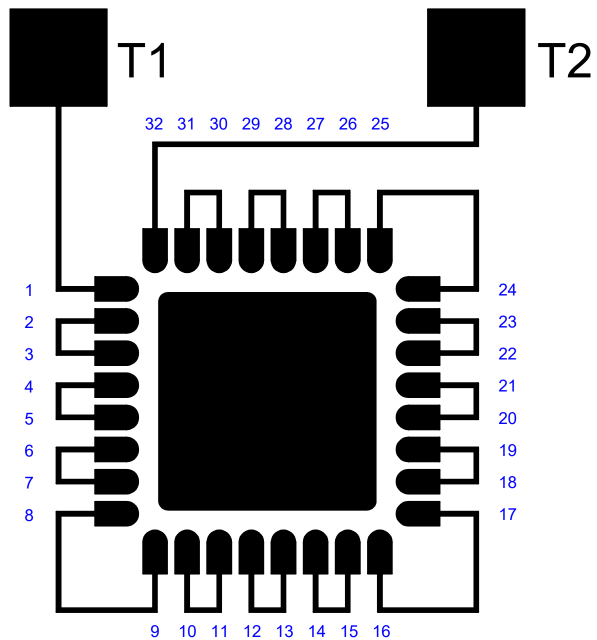


BOTTOM VIEW

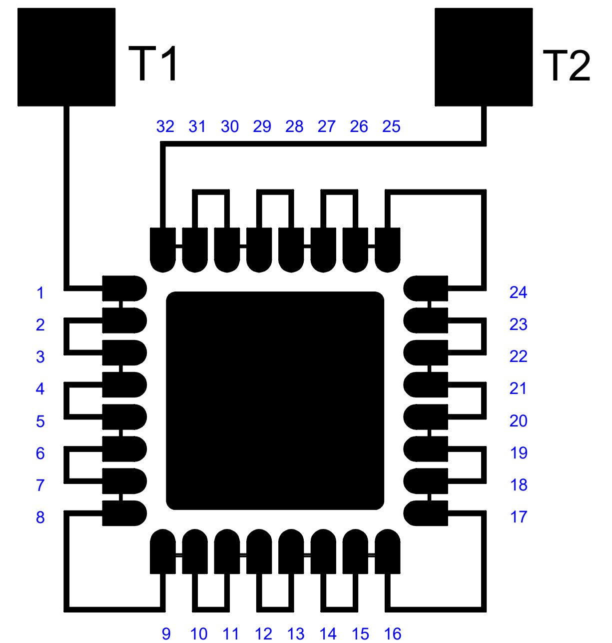


NOTE:
1. PACKAGE DAISY CHAIN BY WIRE BONDING TO INTERNAL BOND PADS.

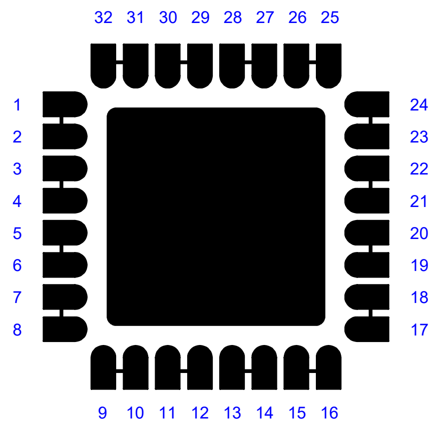
TopLine®			
TITLE	32-LEAD 5mm P=0.5mm QFN PACKAGE		
SCALE 15:1	SIZE A	DRAWING NO. 453238	REV A
DO NOT SCALE DRAWING		SHEET 2 OF 5	



PCB PAD & TRACING



AFTER MOUNTING
QFN ONTO PCB

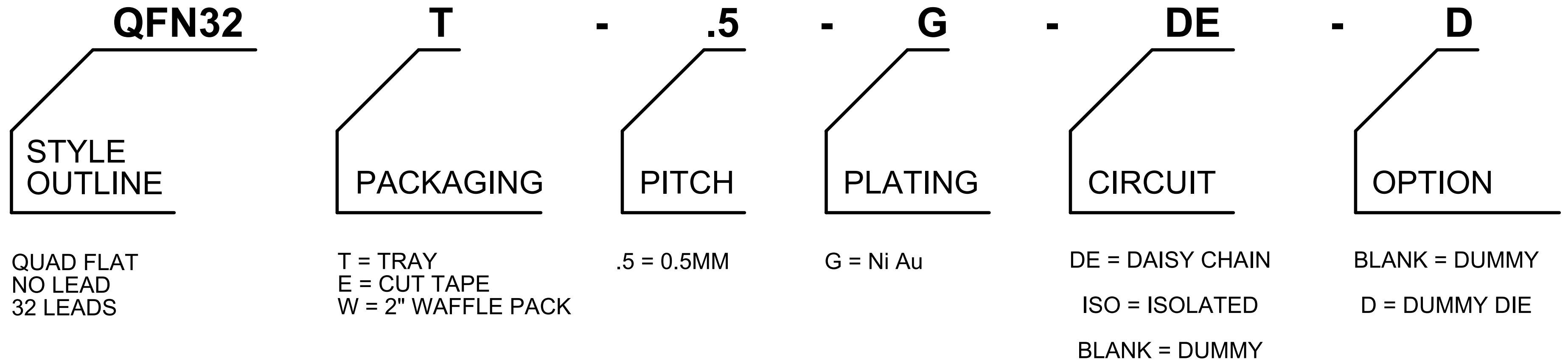


QFN BEFORE MOUNTING

TopLine®

TITLE	32-LEAD 5mm P=0.5mm QFN PACKAGE		
SCALE 8.5:1	SIZE A	DRAWING NO. 453238	REV A
DO NOT SCALE DRAWING		SHEET 3 OF 5	

PART NUMBERING SYSTEM



PART NUMBER	DAISY CHAIN	PACKAGING	RoHS Pb-FREE	DUMMY DIE
QFN32T.5-G-DE-D	YES	JEDEC TRAY	YES	YES
QFN32W.5-G-DE-D	YES	2" WAFFLE	YES	YES
QFN32E.5-G-DE-D	YES	TAPE	YES	YES
QFN32T.5-G	NO	JEDEC TRAY	YES	NO
QFN32W.5-G	NO	2" WAFFLE	YES	NO

OTHER PART NUMBER COMBINATIONS AVAILABLE. CONTACT TOPLINE.

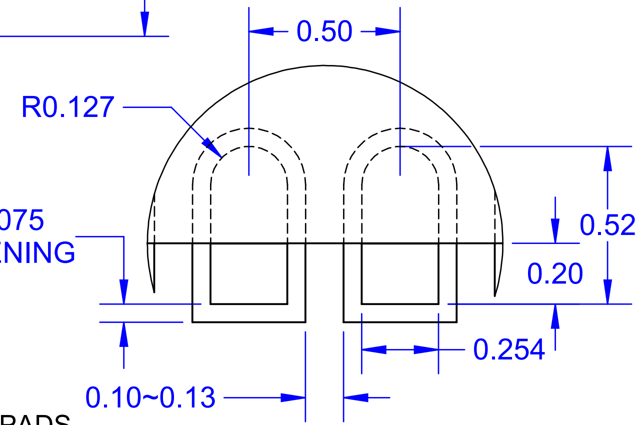
TopLine®

TITLE	32-LEAD 5mm P=0.5mm QFN PACKAGE		
SCALE	SIZE	DRAWING NO.	REV
NONE	A	453238	A

DO NOT SCALE DRAWING

PC BOARD LAYOUT DIMENSIONS IN MM VIEW FROM TOP

5.4
5
3.50
PIN 1
0.50
5
5.4
3.50
0.25
SOLDER MASK OPENING
PCB PAD
COMPONENT PAD
PCB THERMAL PAD
DESIGN OPTIONAL
SEE NOTE 7 & 8
SOLDER MASK OPENING
COMPONENT PAD
3.20
COMPONENT
OUTLINE
A



DETAIL A
SCALE 40 : 1

Notes: (Unless Otherwise Specified).

1) DIMENSIONS ARE PRESENTED ONLY AS A GUIDELINE.
   DESIGNERS SHOULD USE THEIR OWN KNOWLEDGE BASE WHEN DESIGNING THE PCB.
2) SURROUND EACH SIDE OF I/O PERIMETER PADS WITH 0.060~0.075 mm (NSMD) SOLDER MASK
   OPENING (2.4~3.0mils) OPTIONALLY OK TO USE RECTANGLE (NSMD) MASK OPENING AROUND I/O PADS.
3) ROUNDED PCB LAND PADS REDUCE SOLDER BRIDGING. PAD CHAMFER ANGLE MAY VARY.
4) PCB LANDS SHOULD BE 0.2mm LONGER THAN THE PACKAGE I/O PADS.
5) THE WIDTH OF PERIMETER PCB PADS SHOULD MATCH (1:1) THE WIDTH OF THE PACKAGE PADS.
6) REFER TO INDUSTRY REFERENCES SUCH AS IPC-SM-782 FOR PCB LAND PATTERN DESIGN.
7) THERMAL GROUND PADS MAY BE CHANGED TO SUITE REQUIREMENTS OF THE DESIGNER.
   A) MAKE COPPER THERMAL PAD AS LARGE AS POSSIBLE.
   B) DRILL MULTIPLE THERMAL VIAS 0.25~0.33mm DIAMETER USING 0.8~1.2mm PITCH GRID.
   C) PLATE THERMAL VIA BARRELS WITH 1-OUNCE COPPER (18μm).
   D) TENT (COVER) THERMAL VIAS WITH SOLDER MASK 0.1mm LARGER THAN THE VIA DIAMETER.
8) STENCIL DESIGN MAY BE CHANGED TO SUIT REQUIREMENTS OF THE DESIGNER.
   A) LASER CUT STENCIL 0.125mm (5mil) THICK. APERTURE SIZE-TO-LAND RATIO OF 1:1.
   B) THE SOLDER PASTE OPENING IN THE THERMAL PAD AREA SHOULD BE A MATRIX ARRAY OF
   SMALLER APERATURES INSTEAD OF ONE LARGE APERATURE TO CONTROL PASTE AMOUNTS.
   C) APPLY 50% TO 80% SOLDER PASTE COVERAGE IN THE PAD AREA.

TopLine®

TITLE	32-LEAD 5mm P=0.5mm QFN PACKAGE		
SCALE	SIZE	DRAWING NO.	REV
18:1	A	453238	A
DO NOT SCALE DRAWING		SHEET 5 OF 5	