DESIGN PARAMETERS INFLUENCING RELIABILITY OF CCGA ASSEMBLY: A SENSITIVITY ANALYSIS

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ABSTRACT

Area Array microelectronic packages with small pitch and large I/O counts are now widely used in microelectronics packaging. The impact of various package design and materials/process parameters on reliability has been studied through extensive literature review. Reliability of Ceramic Column Grid Array (CCGA) package assemblies has been evaluated using JPL thermal cycle test results (-50°/75°C, -55°/100°C, and -55°/125°C), as well as those reported by other investigators. A sensitivity analysis has been performed using the literature data to study the impact of design parameters and global/local stress conditions on assembly reliability. The applicability of various life-prediction models for CCGA design has been investigated by comparing model's predictions with the experimental thermal cycling data. Finite Element Method (FEM) analysis has been conducted to assess the state of the stress/strain in CCGA assembly under different thermal cycling, and to explain the different failure modes and locations observed in JPL test assemblies.

KEY WORDS: CCGA, solder, reliability, creep, fatigue, thermal cycling, microelectronic package, column grid array.

INTRODUCTION

Advanced IC electronic packages are moving toward miniaturization from two key different approaches, front- and back-end processes, each with their own merits and challenges. Although direct flip-chip die attachment is the most efficient approach for the 2nd level assembly, the area array packages, with balls/columns underneath and irrespective of the die/package ratios, provide ease of die testing at part level. Area array packages such as BGAs (ball grid arrays) and CSPs (chip scale packages) are now widely used for many electronic applications including portable and telecommunication products. The BGA version has been extensively implemented for high reliability applications with generally more severe thermal and mechanical cycling requirements. Extensive work has been carried out by many investigators and the JPL consortia in understanding technology implementation of area array packages for high reliability applications. These included process optimization, assembly reliability characterization, deformation modeling and FEM (Finite Element Model) analysis, and the use of inspection (including X-ray and optical microscopy) and material characterization (including SAM, SEM, Moire') tools for quality control and damage detection due to environmental exposures. Lessons learned by the team have been published elsewhere (1-3).

SOLDER JOINT LIFE PROJECTION MODELS

Significant amount of work has been devoted to life prediction and reliability of tin-lead solder joints used in Ball Grid Array (BGA) and/or Flip Chip. Table 1 lists some of the available models developed for plastic and ceramics grid array packages.

Table 1: summary of various reliability models developed for plastic and ceramic grid array packages.

Model	Reliability/Life-Prediction Representation	Predictive Capability
Coffin-Manson	$N_f = 2.277\times10^{-3}(\text{Max } \varepsilon_{eqv})^{-2.61}$: J. H. Lau	10%-500% inaccuracy
	$N_f = 1.2938(\Delta\varepsilon_{eqv})^{-1.96}$: B. Z. Hong	(expected; since these models are empirical in nature & the constants are determined for a given set of data & conditions.)
	$N_f = 0.4405(\Delta\varepsilon^{eqv})^{-1.96}$: K. N. Chiang, et al.	
	$N_f = K(\varepsilon_p^{-2})$: M. Farooq, et al.	
	$N_f = 0.5(\Delta\gamma/2\varepsilon_f')^{1/C}$: Howieson, M., et al	
	$N_f = 82.4(De_{in})^{-0.863}$: Perkins, A., et al	
Engelmaier	$N_f(x\%) = \frac{1}{2}\left[\frac{2\varepsilon_f'}{F}\frac{h}{L_D\Delta\alpha\Delta T_e}\right]^{-1/c}\cdot\left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{1/\beta}$	>100% (compared to JPL data)
Norris-Landzberg	$AF = \frac{N_g}{N_i} = \left(\frac{\Delta T_i}{\Delta T_g}\right)^{1.9}\left(\frac{f_g}{f_i}\right)^{1/3} e^{1414\left(\frac{1}{T_{max,g}}-\frac{1}{T_{max,i}}\right)}$: S. Y. Teng	
	$N_{50\%} = \left(\frac{100}{\Delta T}\right)^{1.9}\left(\frac{f}{2}\right)^{1/3} e^{1414\left(\frac{1}{T_{max}}-\frac{1}{373}\right)}(G)$	50% (compared to JPL data)
	G=(12439-70.1A-434B-1301C-930D-272E+302CD);	
	A: Substrate size, B: Board & Substrate CTE mismatch	
	C: Substrate thickness, D: Board thickness, E: Ball pitch	
	: A. Perkins, et al	
Darveaux	$N_{init} = C_1(\Delta W_{ave})^{C_2}$, $\frac{da}{dN} = C_3(\Delta W_{ave})^{C_4}$	36%-169% (study by Burmettel)
	C_1 = 13173, C_2 = -1.38 to -1.45, C_3 = 1.72 to 3.92, C_4 = 1.12 to 1.15	
SRS	$N_{63.2\%} / A = C_1(\Delta W_{in})^{C_2}$ C2=-1	Not evaluated, need ΔW values
	: J. Clech	
	$N_f = (\Delta W)^{1.51}\left(\frac{A_i}{A_D}\right)$ A_D=5.9x10-3 mm^2	Wong calibrated Clech model to fit their data!
	: Wong, T. E., et al	
Lall	$N_{1\%f}$=(DietnBcdyRatio)^{b1}(BallCount)^{b2}(BallDiaMM)^{b3} (PCBthkMM)^{b4}(EMCFillID)^{b5}(MaskDefID)^{b6} (BoardFinishID)$^{b7}\Delta T^{b8}$	Note: Impact of temperature is modeled separate from this sensitivity equation.
	$N_{1\%f}$ is the cycle to 1% failure, A and the indices bi's (b1, b2, .., b8) are the coefficients of the model.	

Most of the available models leverage the specific thermal cycling and fatigue test data in developing the constants of the model. Applicability of these life prediction models to other grid array designs and test conditions was investigated by many investigators through independent comparison of models' prediction with the data. Inaccuracies noted are presented in Table 1which mostly are within the 3X expected projection due to the design, process, and test variations. Application of SRS and Darveaux model to CCGA was not investigated in this study due to the lack of inelastic strain energy values used in these models. Detailed inelastic/creep FEM analysis is needed to further evaluate the applicability of these two models to CCGA.

These empirical models are useful tool provided that they are utilized within the realm of the conditions that were used in developing the constants of such models. Extrapolation of such empirical models to conditions outside the boundaries of the model is not generally recommended; as such one may neglect potential mechanism change that may be active in different stress and temperature regimes.

Initial material microstructure and its potential time dependent change/evolution has significant impact on material deformation and failure, hence, affecting package reliability. An integrated reliability tool encompassing the impact of design, processing variables (e.g., variability in cooling rate and composition), and field exposure (e.g., thermal cycling) on microstructural evolution is essential for accurate reliability analysis. Such integrated approach is currently lacking.

Deterministic approach and/or statistical analysis based on worst case scenario are generally used in component life prediction analysis. Such approach which evades the effect of variability in vast number of potential contributing factors (including process/operating variability) renders itself into a non-realistic result. Probabilistic methodology in conjunction with physics-based predictive models is recommended as a mean of incorporating variability.

SOLDER RELIABILITY SENSITIVITY ANALYSIS

The effect of key design and material parameters on solder reliability and the sensitivity analysis is discussed in this section. Extensive bodies of data are published on BGA and CCGA package designs. However, the data reported for CCGA are very sporadic, making the sensitivity analysis based solely on CCGA difficult. In this study both CBGA and CCGA data are leveraged to overcome this problem.

Parametric Study and Sensitivity Analysis

The sensitivity of solder joint reliability on substrate geometry such as thickness (h) and distance from neutral point (DNP) is evaluated using the reported experimental data.

Substrate thickness effect. CBGA data shown in Figure 1 indicate an inverse relationship between the cycle-to-failure (N_f) and substrate thickness, consequence of the increase in substrate stiffness and solders joints loading with the substrate thickness. This behavior is noted for both lead-base and lead-free solder, as shown in Fig. 1.

DNP effect. Increase in Package size (width and length) reduces the N_f, as the DNP (Distance from Neutral Point) and the loading increases. CBGA data indicate a ($1/DNP^2$) dependency on life (see Fig. 2).

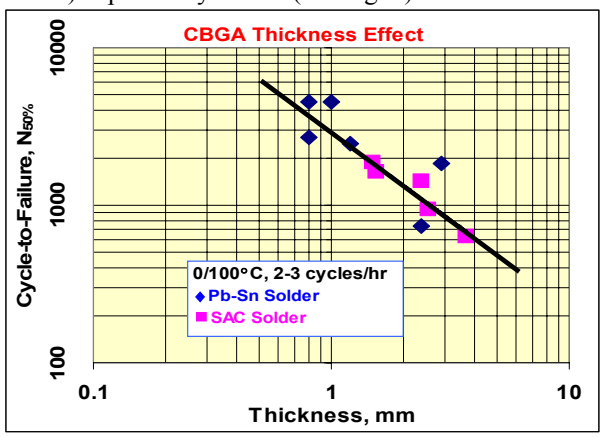


Figure 1. Effect of substrate thickness on cyclic life ($N_{50\%}$)

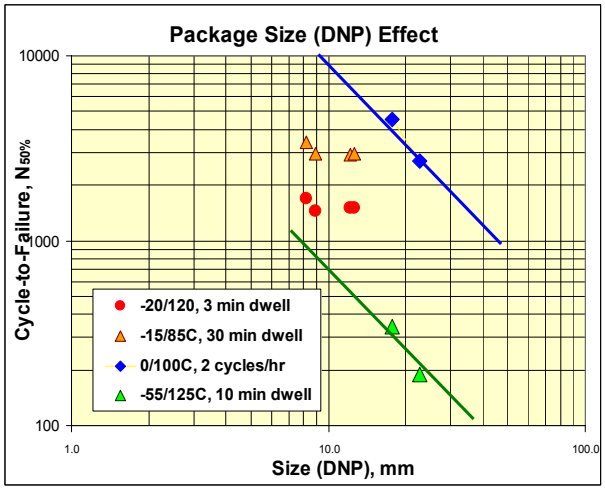


Figure 2. Effect of substrate size on package reliability cyclic life ($N_{50\%}$), for different ATC's

A plot of normalized $N_{50\%}$ life data (normalized to maximum N_f for the population tested at the same ATC), which leverages data generated for different design and at various ATC's, validates the appropriateness of the geometry factor developed in this study (see Fig.3).

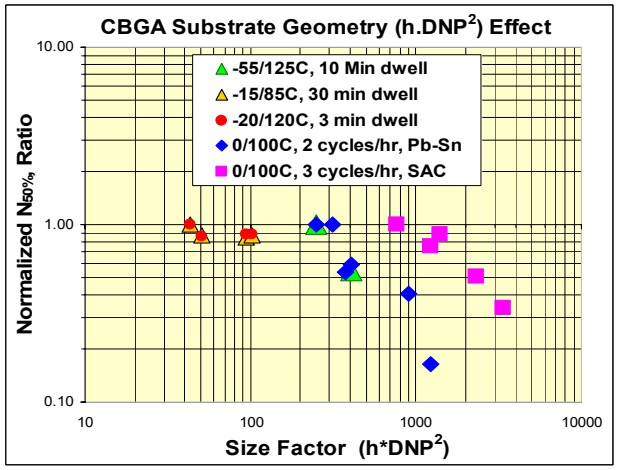


Figure 3. Effect of substrate geometry on cyclic life, for various data generated at different design and test conditions.

Board thickness effect. For PBGA, it is clearly shown that as board thickness decreases, N_f increases. Insufficient set of data was available for any quantitative analysis.

Column height effect. Increases in column height in CCGA package (within acceptable range) improves the reliability due to reduction in solder joint shear strain which impacts the fatigue and creep damage. Insufficient set of data was available for any quantitative analysis, however, a factor of ~4 improvement is noted for CCGA (solder column height of 2.2mm) compared to CBGA (solder Ball height of 0.57mm) packages tested under the same conditions.

Solder volume and substrate pad diameter effects. The effect of these parameters on reliability was investigated by Ghaffarian and others. The reliability of solder joints is expected to increase with standoff gap (solder height) which results in a decrease in joint shear strain, and hence, improved reliability. The effect of solder volume (V), solder bump radius prior to assembly (R), and pad diameters (r_1 & r_o) on solder ball standoff gap (ℓ) is reported to follow the eq.1 below (4).

$$V = \frac{\pi\ell}{6}\left[\ell^2 + 3\left(r_o^2 + r_1^2\right)\right]\ell \qquad ; (1a)$$

$$V = \frac{4}{3}\pi R^3 - \frac{\pi}{3}v^2\left(3R - v\right) \qquad ; (1b)$$

$$v = R - \sqrt{R^2 - r_1^2} \qquad ; (1c)$$

This effect was not quantified due to limited data.

Interposer effect. Addition of interposer to CCGA assemblies showed an improvement in package reliability, reported by Master et al (5), as $N_{50\%}$ life increased from 1520 to 2320 cycles with the addition of Mo-metallized interposer to CCGA packages. However, our recent study which revealed fatigue crack initiation from W-metallized interposer/solder corner/fillet poses an uncertainty on the impact of interposer. Additional work on the effect of interposer metallization layer on solder joint failure is needed to evaluate this effect.

In summary, our analysis of data shows that N_f increases with reduction in substrate thickness, size (DNP), and possibly board thickness; and increases with increase in solder volume, solder/column height, and possibly pad radius.

Effect of Materials/Processing Parameters

Surface finish effect. Board surface; HASL (Hot Air Surface Leveling), ENIG (Electroless Nickel-Immersion Gold), and OSP (Organic Solder Preservative) plays some small role on package reliability. CCGA data reported by Lau (6 & 7) suggest ENIG as the optimum surface finish (see Fig. 4). Lau's data also indicates a small degradation in reliability of lead-free solder with OSP-finish compared to lead-base solder with OSP-finish.

Lead-free solder. Lead-free solders (e.g., Sn-3-4%Ag-0.5-1%Cu) seems to provide a slightly higher cycles to failures for CBGA and PBGA packages at long life (and/or low probability) regime. The effect on CCGA is not clear due to limited data. Properties of lead-free and lead-base solder materials are strongly influenced by the internal structure and morphology of phases and IMCs (inter-metallic compounds) formed during the processing and field exposure. These internal structures are function of material composition, temperature, and cooling rates. Reliability of lead-free solder materials and ATC test results has been reported by many investigators in recent years (7-13). In general improved cycles to failures was reported for SAC alloys [Tin (Sn)-Silver (Ag)-Copper (Cu) alloys], especially for low failure probability regimes. Sensitivity analysis conducted in this study found the impact of SAC to be minor (see Fig. 5).

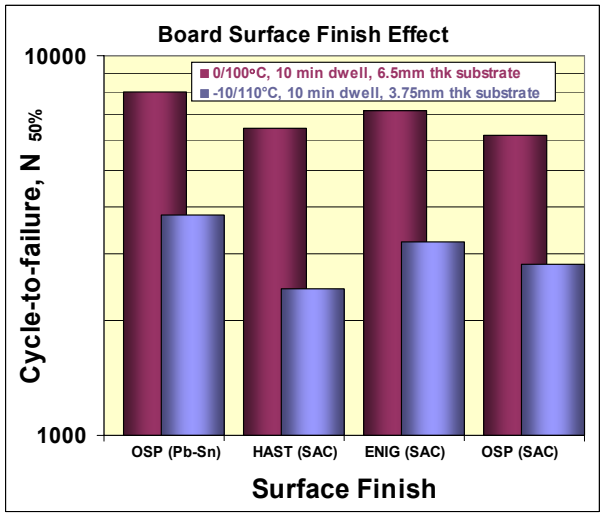


Figure 4. Effect of PCB surface-finish on cycles-to-failure

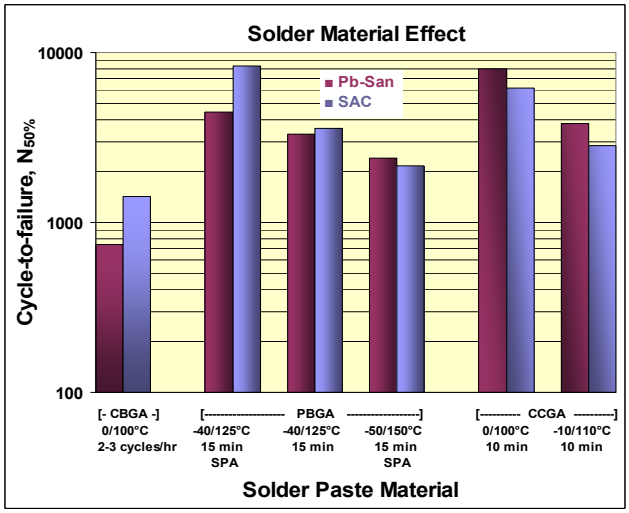


Figure5. Effect of Solder paste material on cycles-to-failure.

In some cases low life or "infant" failure was reported for extreme ATC conditions, e.g., -55°/100°C which is expected when the extreme low temperature level of the ATC is below the DBTT. The data of Ratchev et al. (14) which shows a DBTT value of about -50°C (see Fig. 6) validates this behavior.

Intermetallic compounds effect. Formation of brittle IMC, and its thickness inversely impact package reliability by acting as fatigue initiation sites.

Underfill effect. Addition of underfill material with an appropriate CTE improves the reliability of package by providing a compliant layer to overcome the thermal

mismatch issue. Data generated by Burnettel et al. (15) shows an increase of more than a factor of 2 in life through addition of an underfill material with CTE of 26 ppm/°C.

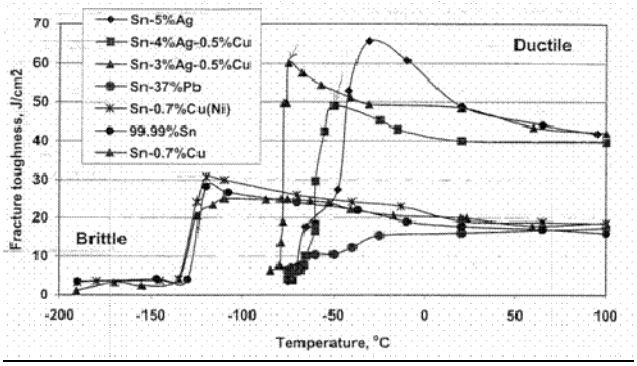


Figure 6. Ductile-Brittle-Transition-Temperature (DBTT) data reported for various solder materials (14).

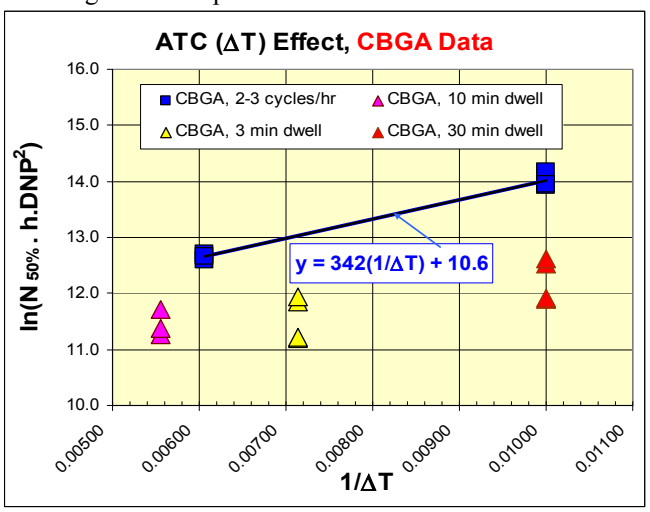
In summary, the data presented in this section indicates that the effect of board surface finish and the industry recommended lead-free SAC on solder joint reliability is small. Presence of IMC's and the solder DBTT strongly influences the package reliability.

Effect of Operation Condition

Temperature cycle and range of operating thermal exposure/condition plays a significant role on reliability due to its impact on loading condition and microstructure evolution and consequent effect on creep and fatigue behaviors. An increase in cycle temperature range (ΔT) and dwell time (t_d) reduces the package life as a result of failure by fatigue (associated with thermal strain induced by CTE mismatch), creep and/or creep-fatigue interaction.

Temperature effect. Effect of ATC temperature range on cycle to failure is presented in Figures 7 for CBGA and CCGA, respectively. The CBGA data used in modeling ΔT effect are associated with possibly 5 minute dwell (2-3 cycles/hr) ATC cycles (5, 16) and the CCGA data have 10 min dwell time (6, 7, 9). A linear dependency between Ln(cycle to failure) and (1/ΔT) is developed leveraging Arrhenius thermally-activated-process model. Note that the cycle-to-failure data in Figures 7 are normalized to geometry factor of $h.DNP^2$ to account for the design/geometry variation in the reported data.

Dwell/hold time effect. Increase in dwell/hold-time during thermal cycling reduces the cycles to failures due to the contribution of creep and its impact on deformation and failure modes. Dwell during the high temperature affects the inelastic strain range, which in turn influences the fatigue and creep life of the component. Grain boundary cavitation due to high temperature creep can also be an active damage/failure mechanism under this condition, as shown later in this study. CBGA data reported by many investigators (15, 17) for T_{max}=100°C (various ΔT's) are presented in Figure 8. Howieson (18) CBGA data generated with 30 min and 3 min dwell times for ATC's of -15/85°C and -20/120°C, respectively, are also shown in Figure 7. A reduction in life with increase in dwell time is obvious from these data. Lack of appropriate data has made the quantitative parametric modeling of the temperature effect difficult.



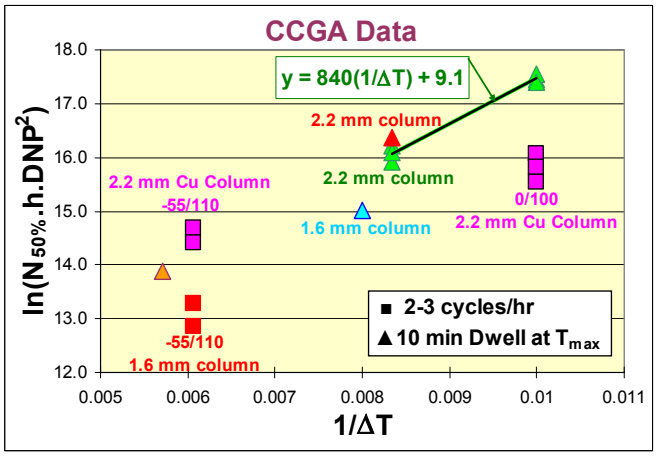


Figure7. Effect of ATC temperature range on reliability

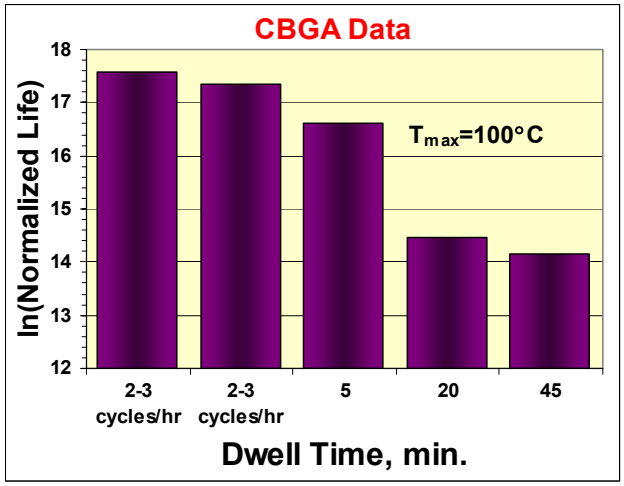


Figure 8. Effect of dwell time on $N_{50\%}$ life for various ATC with T_{max}=100°C. Note that normalized life (adjusted for substrate dimensions and ΔT) are used to account for variation in test samples and conditions.

The lower temperature of a thermal cycle (e.g., T_{min} of ATC) can have a significant effect on reliability, especially

on "infant" failure, if and when this temperature falls below the DBTT of the solder and/or the IMC's. Appropriate material selection with respect to operating condition is the key to avoid this problem. For example, application of current SAC material in space environment, where the T_{min} may fall below -50°C, should be avoided. Figure 6 shows the DBTT data for various solder material, reported by Ratchev (14). Note the DBTT is in -50° to -75°C range for SAC solders (see Fig. 6).

In summary, the operating condition (temperature range and dwell-time) strongly impacts reliability by impacting deformation (inelastic strain) & failure (creep/fatigue/fracture and DBTT effect) of solder joints.

It should be noted that the mathematical functions presented above are for parametric study only and should not be used as a model for reliability predictions at this point. An integrated reliability model incorporating the parameters discussed above is recommended.

MICROSTRUCTURAL AND FRACTOGRAPHIC EVALUATION OF CCGA ASSEMBLIES AFTER THERMAL CYCLES

Samples of CCGA assemblies subjected to two thermal cycle ranges (19); S/N14 (tested @ -50°/75°C, 10 min dwell, for 1819 cycles) and S/N15 (tested @ -50°/125°C, 10 min dwell, for 583 cycles), were evaluated by optical and Scanning-Electron Microscopy (SEM) and Energy Dispersive X-ray (EDX) analysis. Fractographic and metallograraphic analyses were conducted in attempt to identify the failure mechanisms and study the microstructural evolution.

These CCGA packages had 560 I/O's consisting of 0.89 mm diameter and 1.62 mm high 90Pb-10Sn columns (5 peripheral rows) with 1.27 mm pitch in 42.5x42.5x2 mm substrate. The package was staked assembled with W-metallized Al_2O_3 interposer.

Figure 9a and 9b which are low magnification optical photomicrographs of cross-sectioned samples clearly reveal different crack locations noted on these two samples. In both samples the main crack is at the substrate side in solder material, however, these cracks appear at different I/O locations.

The main cracks in S/N14 (-50°/75°C) occur on the columns located in the middle of the peripheral array away from the staked corner, while in S/N15 (-55°/125°C) major crack is located at- and close- to the staked corners. SEM and EDX analysis showed cracks initiating from the interposer/solder fillet, and growing along the interposer/solder interface before transitioning into solder material (see Fig. 10). Increased Interposer metallization layer is noted on S/N15 column, as shown in Figure 11. This effect is being further evaluated.

Grain boundary cavitation indicative of creep mode of failure (along a 45° angle to the column axis, perpendicular to maximum principal stress) was also noted at the substrate side in sample S/N15 exposed to -55°/125°C (see Fig. 12).

Brittle intergranular cracking and solder loss were noted at the board side (and near the staked corners) on S/N15 sample (Fig. 13). The amount of solder loss was lower at the inner columns (lower stresses) and lower temperature S/N14 sample. This observation along with the high magnification SEM/EDX analysis (Fig 13) that reveals the solder loss along the Pb-rich and Sn-rich phase/grain boundaries is indicative of the material loss by grain boundary cracking due to brittle IMC and/or potential creep cavitation/coalescence, and eventual separation/loss.

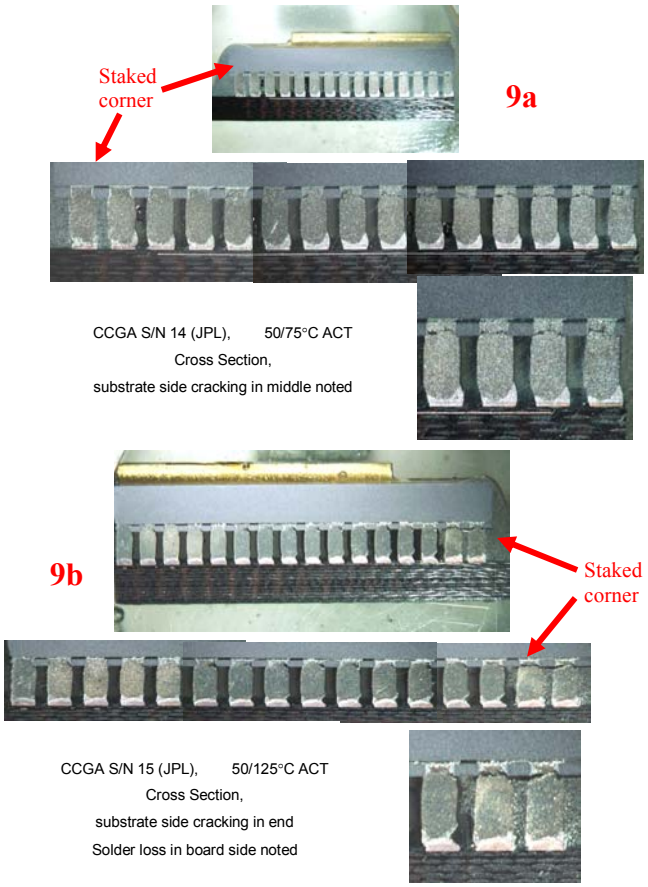


Figure 9. Photomicrograph of (a) -50/75°C and (b) -50/125°C test assemblies revealing crack location and solder loss.

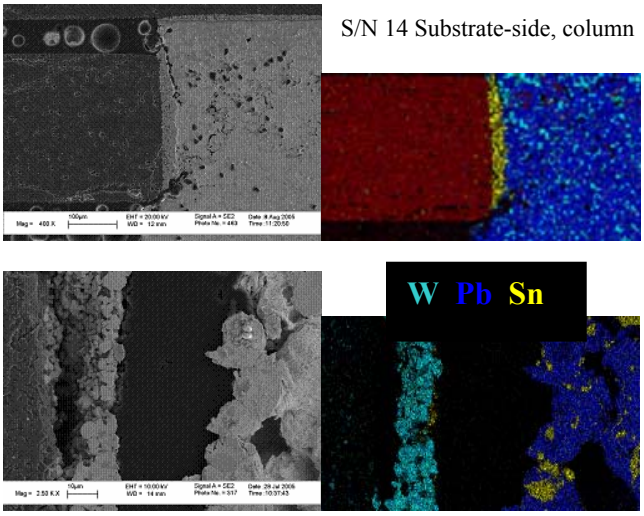


Figure 10. CCGA solder joint crack on substrate side of (a) -50°/75°C, and (b) -55°/125°C TVs initiated from

interposer/solder corner/fillet. EDX clearly reveals crack initiation and growth along the W-solder boundary.

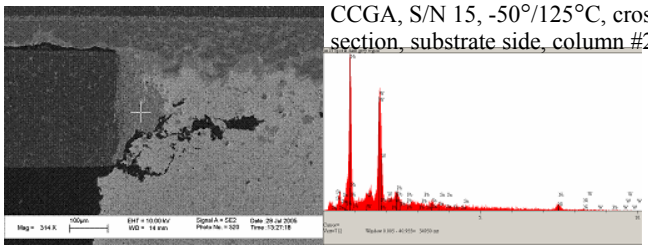


Figure 11. Increased Interposer metallization layer noted.

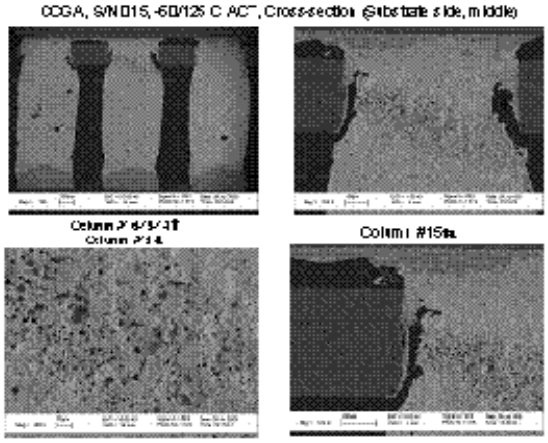


Figure 12. Grain boundary cavitation noted on substrate side solder in -55°/125°C ATC TV.

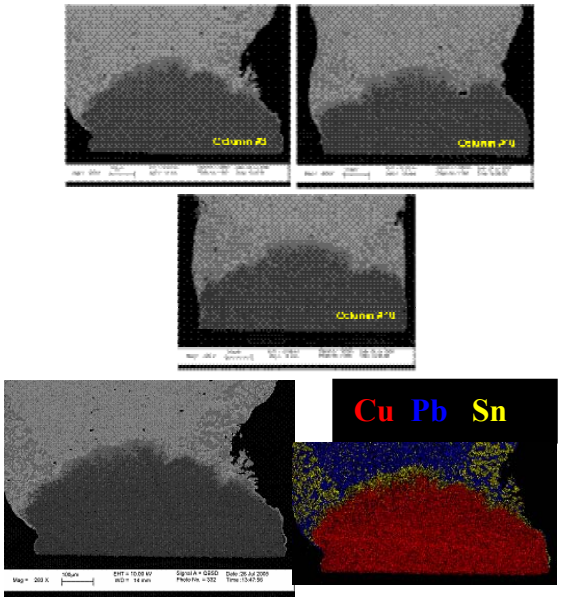


Figure 13. Solder loss and Significant Cu inter-diffusion and IMC formation/growth was noted at board-side solder joints in -50°/125°C ATC (much smaller growth for -50°/75°C ATC).

Fracture Surface Morphology

Samples S/N14 and S/N15 were pulled open and the exposed fracture surfaces were evaluated by SEM in order to investigate the mechanisms responsible for the solder cracking/failure. Fracture surface of solder joints on the substrate side of S/N15 indicated an initial slow crack growth followed by unstable ductile failure. A higher magnification SEM image of S/N15 fracture surface showed the presence of striations, indicative of fatigue mode of solder failure (see Fig. 14).

Substrate side fracture surface of S/N14 revealed somewhat of a different morphology with smaller amount of fatigue and ductile failure zones and more of an intergranular failure. Board-side fracture surface of both specimens (S/N14 and S/N15) showed intergranular morphology with no indication of fatigue failure.

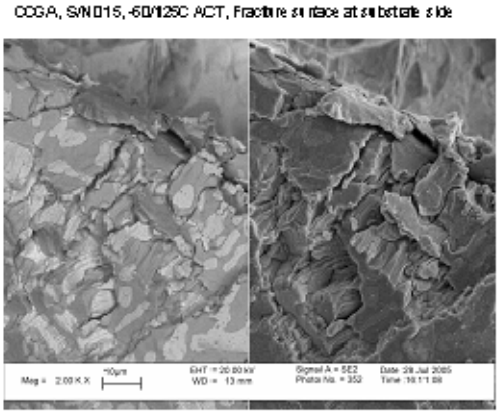


Figure 14. Fracture surfaces of ATC tested CCGA package, indicating fatigue failure at substrate-side of solder joints.

EFFECT OF DESIGN PARAMETERS ON SOLDER DEFORMATION AND FRACTURE

Design parameters such as geometry and application environment which impacts the stress/strain and temperature at solder joint impact the reliability by influencing creep and fatigue behaviors at solder joints. To that end, a preliminary finite element analysis of JPL CCGA samples was carried out.

Preliminary Finite Element Simulations: Macroscopic Model

A finite element model (FE) of the CCGA package was created in ABAQUS® to study the global deformation and stress fields from few thermal cyclic load used for the accelerated tests discussed earlier. By virtue of the symmetry in geometry, loading and material properties, 28307 quadratic hexahedron elements (type C3D20) and 146931 nodes were used to model only half sample and proper symmetry boundary conditions (BC) were applied. Plastic properties were assigned only to the solder, while all other material are hyper-elastic. The latter is the only material modeled as plastic and having temperature dependent properties. No creep rule was considered. The reflow temperature of 220^{o}C was taken as reference temperature for the stress-free configuration of the assembly. To simulate three saw-tooted thermal cycles the package alternated repeatedly between the minimum and maximum temperatures of one cycle, T_{min} and T_{max} respectively. Two cases were analyzed for T_{max}= 75 ^{o}C (case 1) and T_{max} =

125°C (case 2). During a thermal cycle the package experienced increasing stresses during cooling and stress relaxation in the heating phase. Fig.15 shows the stress field in the columns at the end of the first and third cooling respectively for case 1. The first cooling induces the largest stresses. After two thermal cycles the intensity of the stresses is mitigated by the effect of the plastic deformation. This figure shows that, while the three corner columns are unloaded due to the epoxy stakes (not shown), the middle columns are subject to great stresses at the interfaces with the substrate (mostly) and the board. A similar scenario holds for T_{max}= 125°C. Marked plastic deformation occurs in the solder due to load reversal and (kinematic) hardening.

Fig.16 shows the plastic shear strain filed (the ε_{13} component) for case 1 and case 2, which is crucial for the creep and mode II cracking processes. It is evident that the effect of the stakes is to shift the location of maximum shear strain from the corners (which have the largest distance from neutral point "DNP") to the middle columns. The results explain why in case 1 the failure happens in the middle columns. However, the model seems to predict the same scenario also for T_{max}= 125°C. This discrepancy is a model limitation since the epoxy is modeled as hyperelastic and the interfaces are perfect. The simulations show that stakes at the corners experience larger load reversal and higher plastic strains. Under these circumstances, the load-bearing capability of the reinforcements deteriorates rapidly at T_{max}= 125°C and either cracks or creep deformation in the solder can occur at that location due to the large local stresses. Experimental phenomenology of case 2 confirms the occurrence of corner cracks and creep deformation. The glass-transition-temperature of stake epoxy (T_g) may also contribute to this transition in load bearing capability, if T_g is lower than T_{max}= 125°C.

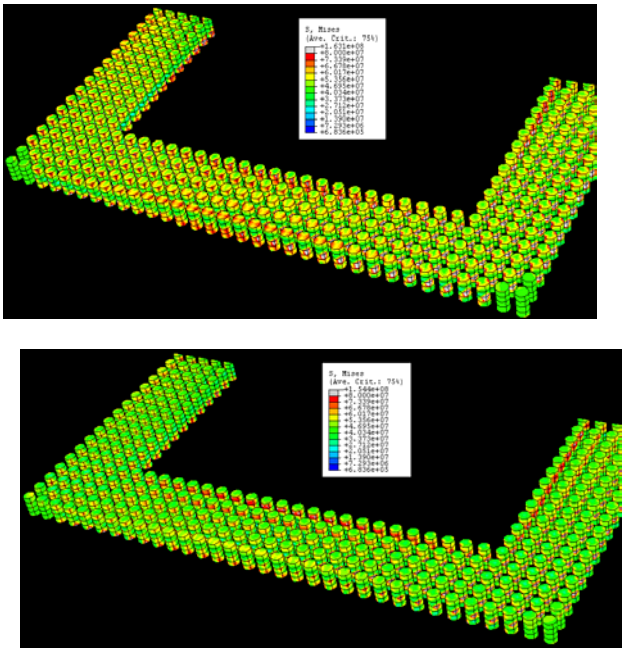


Figure 15. State of stress in the solder columns for case 1 after cooling to T=-50°C in the first (top) and third cycles (bottom).

This analysis clearly shows the fundamental role that the corner stakes seem to play in the transition from one failure mode to another as T_{MAX} changes. A better understanding of the correlation between the reliability of the stiffeners and T_{max} may be beneficial to understand the transition of failure modes. Based on the preliminary results, a more refined version of this model will be developed for a systematic parametric analysis through a better characterization of the material properties. Some of the refinements will aim to include creep rules of solder and to assess the role of corner reinforcements in the failure mode of the package. To this purpose, temperature dependence properties and plasticity will be assigned to the epoxy and other components. These modifications, along with local geometric refinements in the solid model and in the mesh, will also reduce the inaccuracy due to spurious stresses.

Aspects such as microscale stress and strain distributions and the effect of interposer between columns were not assessed with the model. The information provided by this model will be used along with creep deformation models in developing detailed micro-models of local features (say a single column) in investigating microscopic issues at selected critical locations.

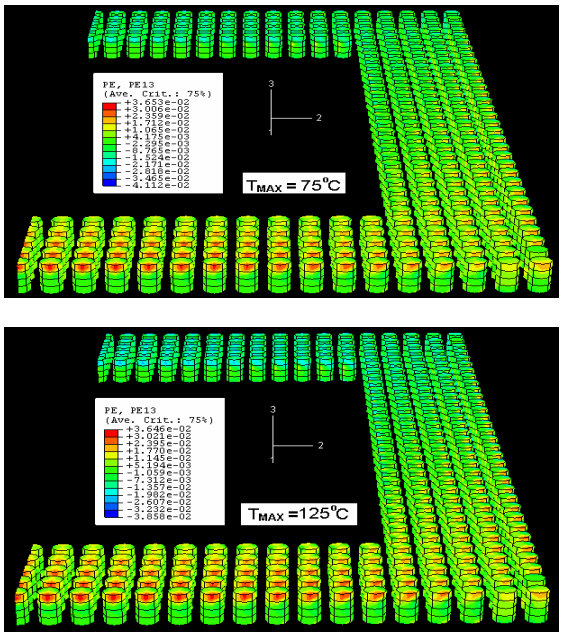


Figure 16. Distribution of the ε_{13} component of the plastic strain for case 1 and case 2, the distributions look very similar.

SUMMARY & CONCLUSIONS

Extensive amount of work have been conducted on flip chip and CSP focusing on reliability testing/analysis, and microstructural evolution. The vast amounts of data generated during decade of study in this field are yet deficient and do not comply with the requirements of IPC-9701A, where key information are not collected/reported in many cases.

The reliability data generated by many investigators on CBGA and CCGA were used in a sensitivity analysis and the

effect of various parameters on reliability of CBGA and CCGA package assemblies was evaluated. A strong temperature, dwell-time, and substrate geometry effect on solder joint reliability was presented. Further analysis based on DoE and DoS along with local/global FEM analysis in conjunction with physics-based deformation and failure mechanisms are recommended for more accurate sensitivity analysis and development of reliability methodology.

Various empirical life prediction models proposed by many investigators for solder joint fatigue failure were evaluated. Inaccuracy of these models in predicting conditions beyond the data used in development of these models reinforces the need for development of an integrated and robust reliability tool/methodology for current and future package designs. Inclusion of the following elements in an integrated/synergistic methodology is recommended:

1. A unified physics-based (or phenomenological) life prediction model, encompassing time-dependent creep, fatigue, environmentally-assisted, and brittle failures
2. A physically based constitutive models representing different solder materials (e.g., lead-free and lead-base), encompassing all potential/active creep mechanisms
3. A Physics-based microstructural evolution model
4. A probabilistic approach addressing variability issues
5. An integrated solution linking all of the above elements and their potential interaction

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