Study of Column Grid Array Components for Space Systems

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INTRODUCTION

This paper addresses the approaches for using Ceramic Column Grid Arrays (CCGAs) in high reliability (Hi-Rel) space systems. While other grid array packaging exist (i.e. Ball Grid Arrays), the part quality (Military "Class S") and radiation hardness requirements of Hi-Rel space systems drive the use of hermetic ceramic components. As will be discussed, the issues of thermal mismatch between ceramic and traditional printed wiring board (PWB) materials requires the use of CCGAs for advanced high pin count digital devices. Unfortunately, even the use of solder column arrays do not provide the same level of solder joint fatigue prevention as traditional compliant gull wing or dual-in-line (DIP) leaded packages. As a result, testing may be required to assure that the CCGA based design meets the wear-out lifetime requirements for Hi-Rel space systems.

Surface mount soldering technologies and accompanying designs for ground based and airborne applications have been trending toward the use of grid array packages (BGAs, CGAs) with ever increasing pin counts, some of which are now greater than 1500 I/O pins. These grid array package configurations provide better signal integrity for higher speed applications required by many of the new Field Programmable Gate Array (FPGA) and Application Specific Integrated Circuit (ASIC) devices. They can also provide better thermal performance, manufacturability, and ease of handling compared to the conventional surface mount leaded parts. Figure 1 illustrates a typical CCGA package configuration compared to a conventional Ceramic Ball Grid Array (CBGA) configuration.

Hi-Rel space applications need to consider these component packaging techniques to increase processing performance and capability. However, there is limited space flight heritage data available for CCGA applications that must survive more than 100,000 thermal cycles. The main reliability problems with grid array devices have been due to solder joint fatigue related issues that arise at the interface to the supporting PWB substrate. This has been shown to be the leading driver for wear-out related failure modes for many applications. Solder joints for component attach can be subjected to a variety of loading conditions (cyclic differential thermal expansion, mechanical shock and vibration) during product life. The coefficient of thermal expansion (CTE) mismatch between the interface of the component and the supporting substrate is another leading driver of solder fatigue.

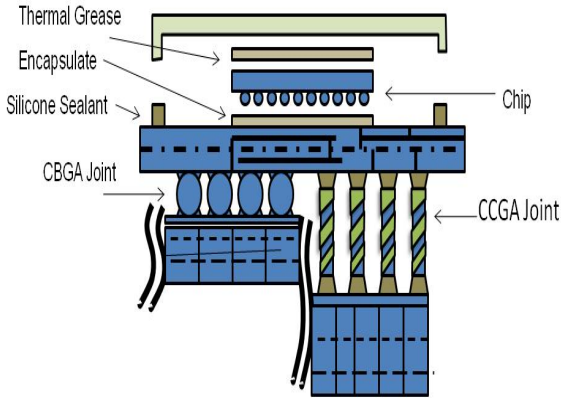

Figure 1. CCGA versus CBGA configurations [1]

As noted, another complication for Hi-Rel space systems is that components are generally required to be hermetically sealed, typically in ceramic packages (per Military requirements). While non-hermetic parts are making some inroads into some Hi-Rel systems, the qualification costs can be prohibitive and often parts rated for high levels of total dose radiation required for space environments are only available with ceramic substrates. There is a variety of Military approved Quality Manufacture List (QML) device types on the market with certified processes for die manufacturing, packaging, and ball grid array attachment. However, these qualifications do not address solder joint fatigue at the interface of the component to the PWB. Without a solid lifetime performance history for a particular design, it's quite common that a reliability test program is required to fully vet the design for the application and to retire the risks associated with this issue.

All Sn/Pb solder joints are susceptible to creep-rupture damage when the solder is placed under any tensional load. Furthermore, when the mechanical loading on the solder joint changes direction, this creep-rupture damage is increased as the solder is essentially "work hardened". Repeated cyclical application and directional changing of the tensional loading on solder joint results in solder joint fatigue. A classic cause of such solder joint fatigue is through temperature cycling of soldered hardware where

there is a difference between the CTE for the part and the support substrate or PWB material. This difference in CTE is known as CTE mismatch. The combinations of temperature changes, due to external environment or power switching, and materials that possess different CTEs, produce substantial cyclic strains within the solder.

SOLDER JOINT FATIGUE

For traditional leaded parts, either Gull Wing or DIP, any board-to-part CTE mismatch is often absorbed by the leads themselves when they are properly formed (known as "compliant leads") and very little tension load is applied to the solder. A practical limit for leaded device pin count is approximately 300 to 350 pins. As noted, to support the increased I/O requirements of current state-of-the-art devices, grid arrays (BGAs, CGAs) have been developed. There is a fatigue concern with grid array attachment because the parts are essentially soldered directly to the PWB with minimal lead compliance to absorb the thermal strain developed by the CTE mismatch between the part and the PWB. When comparing Ball Grid Arrays to Column Grid Arrays, CGAs provide a more robust design for thermal cycling environments by two means

- The solder columns are typically designed to have a lower stiffness than a solder ball (sphere).
- The solder column provides a higher standoff distance between the component and the board.

These two features enable the column leads to flex with less stress as the dimensional expansion between the component and the board varies. The taller standoff will reduce the stress in the solder joint by approximately the square of the distance between the component and the board [2].

While CGAs have slightly higher "lead compliance" than BGAs, the extra lead compliance of the solder column for Ceramic CGAs is often offset by the larger CTE mismatch. Figure 2 illustrates the forces applied to the solder joints resulting from CTE mismatch and thermal excursions and Figure 3 shows an actual failed column joint following temperature cycling.

2.1. Improving Solder Joint Robustness

Matching the CTE as closely as possible reduces cycling stress and improves the reliability of the joints. However, there are tradeoffs between selecting the best CTE compatibility matches and electrical performance. Examples of CTEs for common materials are shown in Table 1.

A method to improve CTE mismatch is to use compatible PWB materials with a CTE closer to the component CTE. One such PWB material is known as Thermount™. Another PWB material is Stablecore™. Conversely, one can also use a ceramic with a higher CTE than the typical alumina compounds (Hi-CTE Ceramic). Unfortunately, not all PWB vendors have qualified processes for the special materials, and not all components are available in the Hi-CTE ceramics. Additionally, there is

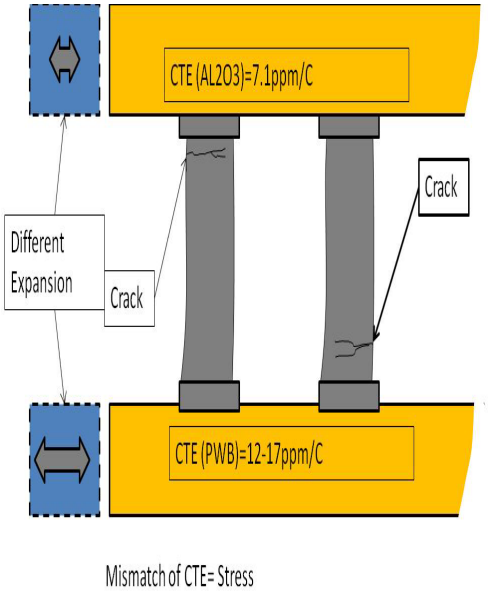

Figure 2. Forces Applied to the solder joints [3]

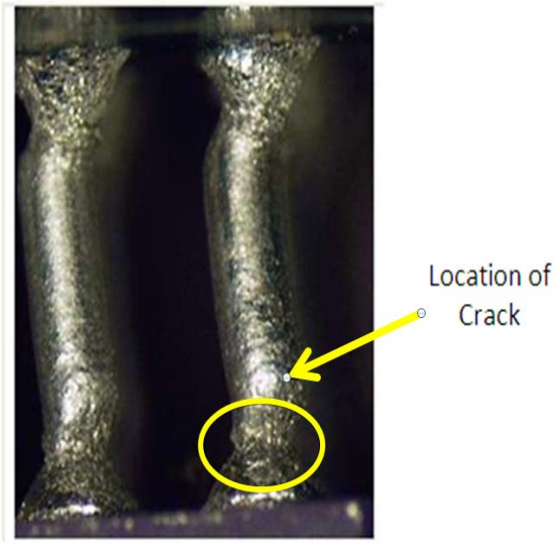

Figure 3. Example of a Failed Column Grid Array [4]

Table 1. CTE for Common Materials[5]

Material	CTE ≈
PLASTIC BGA	15 ppm/°C
Ceramic BGA Material	6.7 ppm/°C
Hi-CTE Ceramic	10 ppm/°C
Polyimide PWB Material	16 ppm/°C

often a mix of component styles on boards and the use of one combination can have adverse effects on the other combination of materials. There are also several kinds of solder columns available in the industry. Some have copper

wire or foil within the columns to provide extra robustness (e.g. 6 Sigma™ solder columns). Figure 4 illustrates some of the features of a 6 Sigma™ solder column.

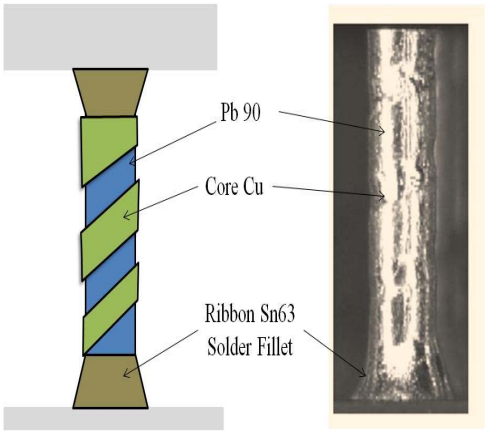

Figure 4. 6 Sigma™ Solder Column Design

2.2. Thermal cycle acceleration models and testing

The fundamental physical issue with space systems is the extended operational mission profiles for each space system, often including over a hundred thousand thermal cycles before end-of-life (EOL). Space systems are exposed to thermal cycling from orbital changes, daily (diurnal) changes, sun angle changes, and power cycling. Since power consumption and mass are critical considerations, they are often continuously power cycled and the circuit board assemblies become a "thermal capacitor", constantly heating and cooling.

As the use of CGAs in space represents a wear-out condition, one means for understanding and mitigating the risk of using CGAs is through the use of thermal cycle life testing. The goal of the accelerated thermal cycle life testing is to determine the wear-out distribution for the CGA/PWB configuration. The resulting onset (e.g. 1% failure rate point) of the wear-out distribution should be greater than the expected number of temperature cycles predicted over life time operation with sufficient margin. Since testing for over 100,000 thermal cycles is prohibitive from both a time and cost perspective, accelerated temperature testing is required. To project an accelerated test to real life, acceleration models were developed. There are several widely known acceleration models used to project test thermal cycles to operational thermal cycles. Two specific models are [6],[7]:

1. The Basic Coffin Manson Model:

$$AF = (\Delta T_{TEST} / \Delta T_{OPERATE})^{2.5} \quad (1)$$

An exponent of 2.4 to 2.5 is used for Sn/Pb solder

2. The Coffin-Manson-Norris-Landzburg Model:

$$AF = [\Delta T_{TEST}/\Delta T_{OPERATE}]^{2.0} (f_{OPERATE}/f_{TEST})^{1/3} \exp(1414\{1/Tmax_{OPERATE} - 1/Tmax_{TEST}\}) \quad (2)$$

where

AF = Acceleration Factor

ΔT_{TEST} = Delta T in the Lab

$\Delta T_{OPERATE}$ = Delta T in the "Field" or "In Use"

$f_{OPERATE}$ = Frequency of cycles in the field (i.e. 16 Orbits / Day - LEO, 1 Orbit / Day GEO)

f_{TEST} = Frequency of test cycles in the lab (i.e. 24 test cycles / day)

$Tmax_{OPERATE}$ = Maximum Temperature in the field

$Tmax_{TEST}$ = Maximum Temperature in the lab

The Coffin-Manson-Norris-Landzburg model addresses temperature dwell times and the absolute temperature within the range of the operational and thermal cycling, but it tends to be more conservative than the Basic Coffin Manson Model. The acceleration factor (AF) for using both equations, as applied to a 5-year space mission, is shown in Table 2. The specific "Life" delta temperature ranges and life cycle quantities are determined from examining the thermal mission profile for a typical "Day In the Life" for the equipment of interest. There are four "life" delta temperature ranges shown with their quantities and expected cycles. Table 2 also shows the results of the 2x and 3x margins as applied to Basic Coffin Manson and Coffin-Manson-Norris-Landzburg model results. It should be noted that a minimum 2x margin should be applied no matter what the case to account for any unforeseen affects.

2.3. Life test accuracy and margin

Several vendors have used similar models to evaluate their CGA designs [8],[9]. Despite the prevalent use of these acceleration models, a wide variability of acceleration results exist for cases where the accelerated test results have been compared to the actual measured thermal cycle fatigue life (wear-out life). Figure 5 reveals this variability. As shown in the graph, there is a noticeable degree of variation between the observed and the predicted acceleration factors.

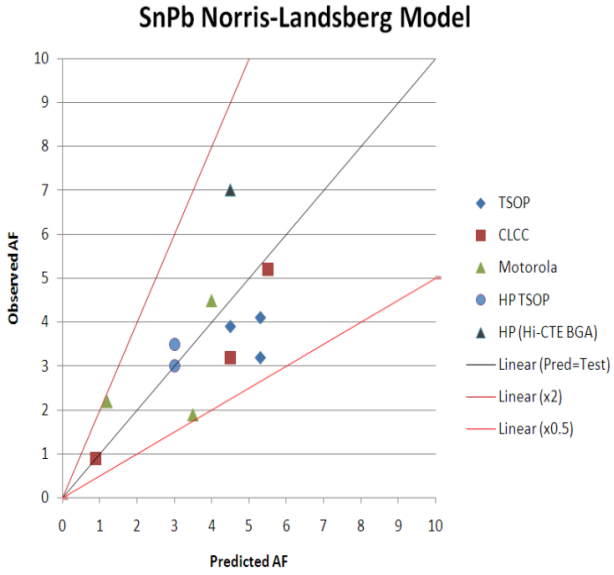

Figure 5. Predicted and Observed Thermal Cycle Acceleration Model results [11]

Based on review of test data versus the predicted values, the true acceleration factors (AF) vary from one-half to twice the predicted acceleration factors. To mitigate this accelerated test variability, it is recommended that a three to four fold margin be applied to the accelerated life results. This margin provides a level of conservatism so that the variability can be discounted. Consultants for NASA specifically recommend applying a three-fold (3x) margin [10].

Table 2. Thermal Acceleration Model

Global Definitions					Exponent					
Test Cycle	Min (Deg C)	-40		C-M	2.5					
	Max (Deg C)	95		C-M-N-L	1.9					
	Delta T	135								
	Lab Cycles/Da	4					Basic Coffin-Manson		Coffin-Manson - Norris - Landzberg	
Item	Years	Cycles / Day	Total Cycles	Tact max	Tact min	Delta T	AF	Test Cycles	AF	Test Cycles
Manufacturing/ESS	0.276	0.1	10	80	-20	100	2	4.757	1	17
Integration/Test	0.276	0.15	15	45	15	30	43	0.352	11	1
Life - 0-5C DT	5	17	31025	41	39	2	37433	1	9378	3
Life - 6-10C DT	5	21	38325	38	35	7	13584	3	4864	8
Life - 11-15C DT	5	20	36500	48	33	15	243	150	195	187
Life - 16-20C DT	5	6	10950	50	30	20	118	93	74	149
		Total	116825			1X	Total	251		365
						2X	Total	503		730
						3X	Total	754		1095

2.4. Recommendations for cga thermal cycle life testing

There are several recommendations for CGA thermal cycle life testing. These recommendations are advised for any accelerated life test. One of the most important (especially for larger CGA styles) is that thermal cycle life testing be performed for each CGA style mounted to a PWB that represents the final configuration to the maximum extent possible. The life testing should use the exact package and board mounting configuration and physical properties, including package size, internal die size, ball material size and pitch, solder mask, and PWB stack-up (thickness, layers, etc) used in the actual package. If the exact configurations cannot be tested, IPC-9701, Table 4-3 (Test Exemption Requirements) can be used as a guide to determine the extent of the allowed configuration deviations. IPC-9701 should be used to define the life test conditions and required sample sizes. The accelerated life test thermal cycle profile should be based upon initial startup conditions and the operational temperature levels anticipated at the components interconnection interfaces. The dwell duration at the extremes shall be a minimum of 15 minutes. This dwell time provides sufficient time for the solder to "creep" or deform under tensional load. Per IPC-9701, the sample size of each device type shall be 33 devices, 32 for life test and one for cross-section. All testing should be performed using "Daisy Chained" parts and PWB interconnections so that continuous continuity monitoring can be performed with an IPC approved event detector. The temperature rise from chip self heating should be reflected in the predicted thermal cycle numbers. Therefore, differences between the actual chip and daisy chained chip need to be considered. The "Daisy Chained" parts should reflect the exact part configuration (size, materials, layer count, thickness), with the exception that the I/O be connected in a fashion allowing for a complete daisy chained interconnection to a properly designed daisy chained PWB. The corresponding Daisy chain PWB design should have the same copper and insulating layer stack up as the actual board design, again with the exception that the circuitry connection to the parts be designed to have continuous daisy chained continuity loops. The resulting PWB and component assembly should be performed using the identical soldering and assembly processes as the final product.

2.5. Space program CGA thermal life testing

The following is an example of a CGA evaluation test. As illustrated in Table 2, a Day-In-The-Life thermal cycle mission profile was created. Using the Basic Coffin equation, an equivalent accelerated life test value of 251 cycles (-40°C to +95°C) was computed as the "1x" lifetime value (no margin). The application required a "3x" margin for wear-out distributions, therefore, the resulting CGA thermal life test cycle requirement was determined to be 754 cycles. The complete mission profile includes contributions from manufacturing/screening, Integration/Test and on-orbit "life" temperature cycling as shown in Table 2.

An Event Detector (Analysis Tech™, STD Series) monitored each solder joint during test. The test boards began to show CGA failures (open circuits) at 879 test cycles (refer to Table 3). The primary objective of the test program followed by the Weibull analysis is to determine the Column

Grid Array (CGA) life. As noted, the time to first Failure was 879 Test Cycles. However, an important criterion is the 1% failure point on a Weibull plot as shown in Figure 6. For the full set of data, the 1% failure point was 740 Cycles.

Table 3. Test Board Results

	Data Channel	Component	Circuit	Bd Serno	Cycle Count
1	81	U3	# 5	7	879
2	145	U3	# 5	12	912
3	5	U3	# 5	1	933
4	69	U3	# 5	6	960
5	17	U3	# 5	2	968
6	169	U3	# 5	14	969
7	117	U3	# 5	10	981
8	157	U3	# 5	13	1042
9	41	U3	# 5	4	1083
10	93	U3	# 5	8	1083
11	53	U3	# 5	5	1102
12	133	U3	# 5	11	1107
13	29	U3	# 5	3	1155
14	181	U3	# 5	15	1182
15	105	U3	# 5	9	1184
16	197	U3	# 5	16	1232
17	129	U1	# 1	11	1293
18	89	U1	# 1	8	1326
19	177	U1	# 1	15	1362
20	153	U1	# 1	13	1370
	---Data Continued---				

However, careful analysis of the data revealed dual slopes, which indicates a Bi-Modal distribution. Confidence of the dual slopes is confirmed by the fact that the Coefficient of Determination (r^2) factors of the individual data plots are higher than the combined plot, and the early failure mode plot has an extremely high Coefficient of Determination value of 0.95. Since the time to first failure is the most important, only the earliest failure mode distribution is used to determine the minimum design life. Plotting the earliest failure mode distribution shows a beta (□) of 30.1, which is strongly indicative of a wear-out related phenomenon. Since the 1% point of 820 test cycles was above the 754 cycle goal, the life requirement (with a 3x margin) was satisfied and the overall design was deemed suitable for its application.

2.6. Other test programs and studies

In recent years, various board level thermal cycling qualification programs have been conducted by several device vendors. Two notable test programs were performed by Xilinx and Actel Corporations in support of their CGA designs. Although those test programs showed mixed results that varied depending on the given configurations, both test programs indicted the CGA designs have the capability to meet the needs for many space programs [12],[13].

CONCLUSION

A good reliability test program to evaluate solder joint fatigue risks should be implemented with the goal of confirming the design meets the service life requirements of the application. In particular, it should be focused on reflecting the lifetime temperature cycling exposure the equipment is expected to experience across the expected life. Subsequently, the environment and design life requirements must be fully analyzed and understood up front. An accelerated life test can be effectively designed using the Basic Coffin Manson model. This approach can be used to derive acceleration factors to use in designing a robust test program.

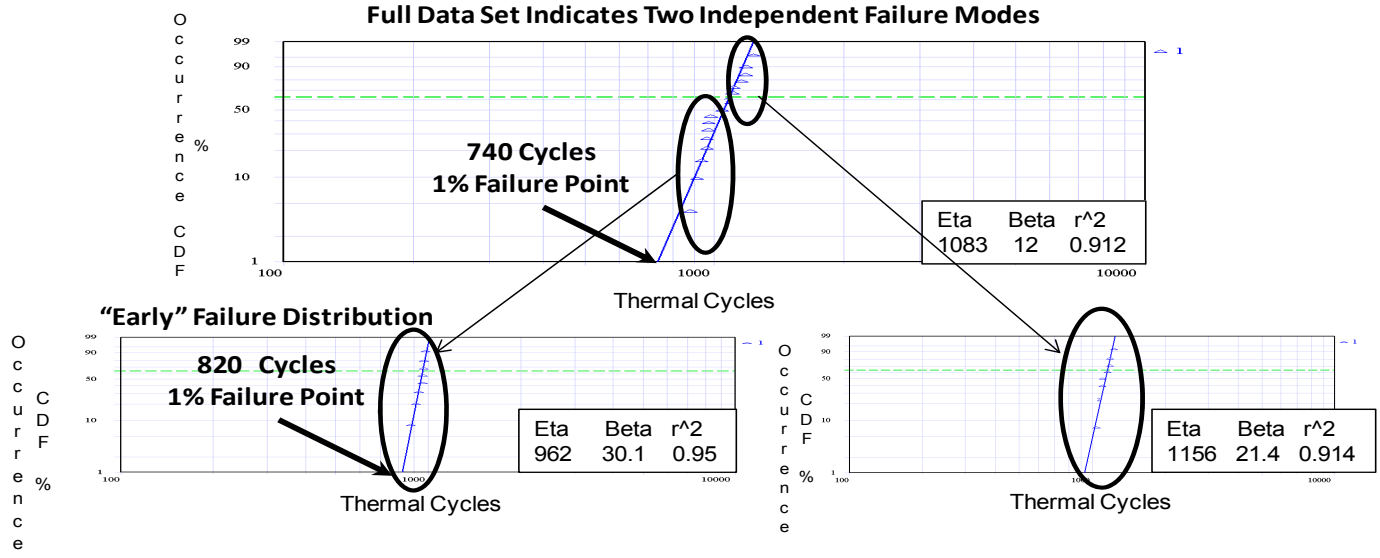

Figure 6. Weibull Plotted Test Data

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