Thermal Testing of a 3-Die Stacked Chip Scale Package Including Evaluation of Simplified and Complex Package Geometry Finite Element Models

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Abstract

Thermal performance testing was conducted on a 16x16mm, 2-metal layer, 591-ball, 0.50mm pitch, 1.20mm overall height Chip Scale Package (CSP) containing an offset pyramid configuration of three stacked Delco thermal test die. Die sizes from bottom-to-top were 10.16x10.16mm (Delco PST-6), 6.35x6.35mm (Delco PST-4), and 3.81x3.81mm (Delco PST-2). Testing was carried out using eight different multi-die power configurations in a natural convection environment to highlight the effects of radiant and convective heat transfer. Measured data was obtained on a sample size of five packages to calculate Theta JA, Psi JT, and Psi JB values at each of the eight different multi-die power configurations. Furthermore, Theta JC and Theta JB cold plate measurements were also obtained. For the purposes of thermal testing, each of the five CSP test samples was mounted on a JEDEC standard 101.5x114.1x1.60mm 1S2P thermal test board. Measured results are used to suggest a methodology for the generation of linear superposition matrix equations as a means to present multi-die package thermal test data such that it may account for changes in thermal cross talk between die at varying die power configurations.

The ANSYS finite element analysis modeling software was used to simulate the eight aforementioned thermal test configurations for the purpose of verifying the acquired test data. Both simplified and complex package substrate metal layer trace patterns were evaluated for simulation accuracy. The simplified patterns consisted of conductor traces that do not follow the detailed routing of the actual design, but instead extend straight outward towards the substrate edge. Alternatively, the complex patterns consisted of the detailed trace layers exactly as they are physically routed on the CSP substrate. In both the complex and simplified metal layer trace pattern finite element models, vias that connect the top and bottom trace layers were represented by two-dimensional thermal conduction elements. Simulated results for both the simplified and complex metal layer trace pattern models are compared to the acquired test data. The CSP package structure, thermal test data, and finite element models are presented and discussed.

1. Introduction

In many applications the thermal performance of a packaged semiconductor device is measured by a lumped steady-state junction-to-reference thermal resistance value based on a single heat source configuration. This lumped thermal resistance value, designated $R_{\theta JX}$ or simply θ_{JX}, relates the temperature rise of a packaged integrated circuit (IC) junction above a reference temperature when a known constant power is dissipated from the die. This thermal resistance, represented by the Greek symbol Theta, is commonly defined by the equation

$$\theta_{JX} = \frac{T_J - T_X}{Q_{JX}} \quad (1)$$

where T_J is the junction temperature, T_X is the reference temperature, and Q_{JX} is the power which flows only between the junction and reference temperatures. In most cases the reference temperature is either the ambient temperature (θ_{JA}), the top temperature of the package case overmold (θ_{JC}), or the test board temperature in direct proximity to the package edge (θ_{JB}). For Theta JC and Theta JB values, the package case and test PCB are connected to a cold plate to force the power (or heat) to flow from the die to the point of reference. However, it is common for case and board temperatures to be acquired during forced or natural convection testing where a cold plate is not utilized. Thus, the power that flows only between the junction and reference temperatures becomes unknown, requiring the use of a known power such as that applied to the die. Since the power in the denominator of Equation (1) is no longer that which flows only between the junction and reference temperatures given in the numerator, the calculated value is no longer a true "thermal resistance" value, but instead is a "thermal reference" value represented by the Greek symbol Psi as follows:

$$\Psi_{JX} = \frac{T_J - T_X}{Q_{Die}} \quad (2)$$

Multi-die packages, where several power dissipating devices reside within the same package structure, do not fit into the simple thermal models represented by Equations (1) or (2) as they assume one reference junction, one heat source, and cannot account for the thermal crosstalk between die. In many cases this fact is ignored and devices are lumped together to generate an average steady-state thermal resistance value, as was the approach of Bar-Cohen [1]. However, as Bar-Cohen noted, this technique can only be applied if the die are of identical geometry and power dissipation. An alternative to this approach is the utilization of a die location specific thermal resistance which is defined in terms of the local power dissipation of the individual devices. This approach was discussed by Sullhan et al. [2] but was

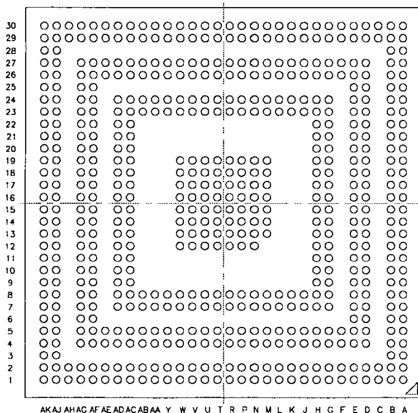

Fig. 1. Solder ball matrix.

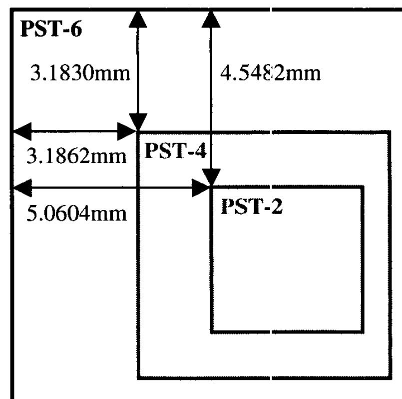

Fig. 2. Stacked die configuration.

found by Kromann [3] to be impossible to apply in situations where specific devices are left unpowered.

Each of these methods of thermal characterization attempt to compensate for some fundamental thermal physics, specifically that unless all devices in the package structure are always powered in fixed relative proportion, their thermal path to the reference temperature (T_X), whether it is lumped or individualized for each power dissipating die, cannot be represented by only a simple thermal model as commonly incorporated in the electronics industry through the utilization of Equations (1) and (2). A more sensible approach to the problem of characterizing the thermal performance of multi-die packages is to acknowledge the multiplicity of junctions and heat sources that exist within the package. Although the resulting model is somewhat more complex to measure and apply to system level thermal analysis, it does provide a more accurate steady-state thermal prediction of the multiple devices within the package structure.

Studies by Aghazadeh and Jain [4], Lall et al [5], and Sofia [6] utilized the principle of superposition to generate a linear thermal resistance matrix equation that can then be solved over a range of multiple die power configurations. As was noted by Sofia, this approach has its limitations due to systematic errors caused by radiation and convection induced non-linearities that are most evident in a natural convection environment. Inherent non-linearities due to thermal conductivity material properties can also introduce errors when linear superposition is utilized as a package thermal characterization method. A study by Zahn [7] incorporated a statistical approach whereby response surface equations were generated to evaluate the thermal interacation between three die orientated side-by-side in a multi-die plastic ball grid array (PBGA) package. This methodology was found to nicely account for convection and radiation induced non-linearities along with temperature effects on thermal conduction material properties. However, it has the small disadvantage of requiring the utilization of a statistical fit software tool and tends to result in somewhat cumbersome equations.

All of the aforementioned studies have one commonality in that each of the packages evaluated incorporates side-by-side die configurations, thus creating a greater die-to-die thermal disconnect than is experienced in stacked die configurations like that of the package evaluated in this study. Thus, the accuracy of describing the thermal performance of a stacked die package using both an average lumped steady-state thermal value, as defined by Equations (1) and (2), and using the principle of superposition are re-evaluated. Furthemore, finite element simulations are performed to verify the results of the acquired thermal test data, including a comparison between finite element models that incorporate simplified and complex package substrate metal layer trace patterns. The routing of conductor traces in a laminate based substrate package design, including their width and spacing, effects the packages ability to spread and dissipate heat. Therefore, conductor trace routing will effect the overall thermal performance of the package and needs to be properly represented in the finite element models to insure the accuracy of the simulated results.

2. Package and Test PCB Description

A 16x16mm, 2-metal layer laminate substrate (approximately 0.21mm thick), 591-ball (0.50mm pitch), three die stacked chip scale package was evaluated. The ball configuration consisted of a 30x30 full matrix with selected rows of balls depopulated as shown in Figure 1. The overmold was 0.70mm thick and had the same XY dimensions as the package substrate (16x16mm). Delco PST-2 (3.81x3.81mm), PST-4 (6.35x63.5mm), and PST-6 (10.16x10.16mm) thermal test die were stacked from top to bottom in an offset pyramid configuration as shown in Figure 2. All three die were background to 0.127mm thick and utilized a die attach material that was 0.0381mm thick. Note that the bottom die (PST-6) utilized electrically conductive die attach material whereas the center and top die (PST-4 and 2 respectively)

utilized non-electrically conductive die attach material. This is important to note as the electrically conductive die attach material has a thermal conductivity 5X greater than non-electrically conductive die attach material. All three Delco thermal test die meet the requirements of JEDEC specification EIA/JESD51-4 [8]. A 0.30mm diameter solder ball was used resulting in a substrate reflow standoff height of 0.22mm. The 2-metal layer substrate stackup consists of top and bottom solder resist layers 0.030mm thick each, top and bottom metal (or trace) layers 0.022mm thick each, and a core laminate layer that is 0.100mm thick.

Each of the five package samples was tested after reflow to a 101.5x114.5x1.60mm 1S2P thermal test PCB per JEDEC specification JESD51-9 [9]. The test PCB stackup consists of top and bottom solder resist layers of 0.035mm thick, top and bottom trace layers of 0.070mm thick, top and bottom pre-preg laminate layers 0.440mm thick, and a core laminate layer that is also 0.440mm thick.

3. Thermal Performance Test Description

Natural convection thermal testing was conducted within a $0.0283m^3$ chamber per JEDEC specification EIA/JESD51-2 [10]. As previously mentioned, the test sample size was five units. A thirty-six gauge K-type thermocouple was attached to the top center overmold of each package for the purpose of Psi JT measurements. Furthermore, a K-type thirty-six gauge thermocouple was attached to a trace on the top of each PCB, centered along the length and within close proximity to the package body edge, for the purpose of Psi JB measurements. Thermocouple adhesion was achieved using Thermalloy Thermalbond 4951 thermally conductive epoxy material.

Prior to testing, each Delco thermal test die was calibrated against a thirty-six gauge K-type master thermocouple using a 0.50mA diode measurement current. All attached thermocouples were also calibrated against the same master thermocouple. A Delta Design 9023 oven was used for all diode and thermocouple calibrations. Delco test die diode voltages and attached thermocouple temperatures were fit to the master thermocouple temperature using a quadratic model ($T=C_0+C_1X+C_2X^2$; where T is temperature in °C and X is voltage for Delco test die diodes or temperature for attached Psi JT and Psi JB thermocouples). The root mean square errors for the quadratic fits ranged from 0.008-0.112°C.

Figure 3 displays a JEDEC standard natural convection test chamber setup. The previously mentioned master thermocouple used for calibrations was positioned within the test chamber per JEDEC specification EIA/JESD51-2 [10] to measure the temperature of the ambient air. A ribbon cable linked the PCB edge connector socket pins to an Agilent E3631A multiplexer data acquisition unit used to collect voltage, resistance, and temperature data. Power to the three Delco thermal test die was provided by an Agilent 6629A quad power supply, thus allowing each of the three stacked die to be separately configured to any variety of power levels.

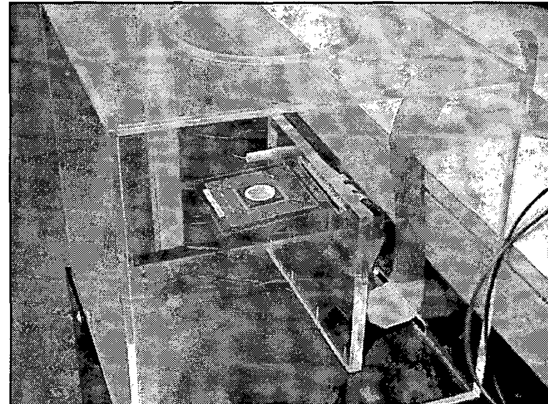

Fig. 3. JEDEC standard natural convection test chamber setup.

Further testing was performed to obtain both Theta JB and Theta JC measurements. Theta JB testing was conducted using a ringed cold plate per JEDEC specification JESD51-8 [11]. Theta JC testing was conducted using a flat cold plate. An enhanced thermal connection between the package overmold and cold plate was facilitated through the utilization of Dow Corning 340 heat sink compound (i.e. thermal grease) during Theta JC testing. Note that a JEDEC specification for Theta JC measurements currently does not exist. Theta JB and Theta JC measurements utilized a NESLAB RTE-111 heat exchanger to cool the fluid that flowed through the cold plates. The calibration master thermocouple used for ambient temperature measurements during natural convection thermal testing was applied to measure the cold plate temperatures during Theta JB and Theta JC testing.

For each thermal test, power was applied to the test die and the package and PCB were allowed to thermally stabilize at which point temperature and power data was collected. Internally developed National Instruments LabView programs communicated with the thermal test instrumentation through their respective IEEE-488 interface bus ports, thus automating all of the described thermal testing. Steady-state conditions were verified by plotting die power and junction temperatures, along with attached thermocouple temperatures, versus time. Acquired steady-state ambient temperatures ranged from 21.4 to 22.9°C for the eight different multi-die power configurations tested.

4. Thermal Performance Test Data and Generation of Linear Superposition Matrix Equations

Tables 1 and 2 summarize the averaged results of the natural convection and cold plate thermal testing respectively. The largest standard deviation was

Table 1. Theta JA, Psi JT, and Psi JB Natural Convection Test Data

Test	Power (W)				Theta JA (°C/W)			Psi JT (°C/W)			Psi JB (°C/W)		
No.	PST2	PST4	PST6	Q_{Totl}	PST2	PST4	PST6	PST2	PST4	PST6	PST2	PST4	PST6
1	2.50	0.00	0.00	2.50	35.9	30.5	24.9	9.6	4.2	-1.4	22.6	17.2	11.6
2	0.00	2.50	0.00	2.50	28.3	29.1	25.5	2.7	3.5	-0.1	14.7	15.6	11.9
3	0.00	0.00	2.50	2.50	22.3	23.0	23.7	0.6	1.3	1.9	9.6	10.3	11.0
4	0.25	0.25	0.25	0.75	29.7	29.7	27.5	6.8	6.9	4.7	15.7	15.7	13.5
5	0.50	0.50	0.50	1.50	28.7	27.9	25.4	6.7	5.8	3.3	15.4	14.6	12.1
6	0.75	0.75	0.75	2.25	28.7	27.5	24.9	6.8	5.6	2.9	15.5	14.3	11.6
7	1.00	1.00	1.00	3.00	28.7	27.4	24.5	6.9	5.6	2.8	15.6	14.3	11.5
8	1.25	1.25	1.25	3.75	28.6	27.2	24.3	7.0	5.6	2.7	15.7	14.3	11.4

Table 2. Theta JC and Theta JB Cold Plate Test Data

Test	Power (W)				Theta JC (°C/W)			Theta JB (°C/W)		
No.	PST2	PST4	PST6	Q_{Totl}	PST2	PST4	PST6	PST2	PST4	PST6
1	2.50	0.00	0.00	2.50	10.3	6.8	4.2	22.2	16.8	11.5
2	0.00	2.50	0.00	2.50	5.5	7.2	5.2	14.6	15.4	11.9
3	0.00	0.00	2.50	2.50	3.1	4.2	5.3	9.8	10.5	11.1
4	0.25	0.25	0.25	0.75	7.0	7.6	6.6	15.6	15.4	13.4
5	0.50	0.50	0.50	1.50	6.4	6.5	5.4	15.4	14.5	12.0
6	0.75	0.75	0.75	2.25	6.3	6.1	5.0	15.4	14.2	11.5
7	1.00	1.00	1.00	3.00	6.2	5.9	4.7	15.5	14.1	11.4
8	1.25	1.25	1.25	3.75	6.1	5.8	4.6	15.6	14.1	11.3

calculated as 0.43°C/W and occurred in the Delco PST-2 die during Theta JB cold plate test number 8 for which the average Theta JB value was calculated as 15.6°C/W. All acquired test data indicated standard deviations that were at least a magnitude of order less than the averages. Note that the Theta and Psi values were calculated as shown in Equations (1) and (2) respectively. However, the denominator was the total sum of all three die powers as also provided in Tables 1 and 2. Eight thermal tests were performed in order to create a linear superposition matrix equation including the addition of a non-linear matrix multiplier.

Without belaboring the math, a linear superposition matrix equation that can be used to estimate multi-die junction temperatures for multi-die power configurations can be derived and is shown in Equation (3).

$$[Q_0 \quad Q_1 \quad Q_2] \bullet b \bullet \begin{bmatrix} R_{00} & R_{01} & R_{02} \\ R_{10} & R_{11} & R_{12} \\ R_{20} & R_{21} & R_{22} \end{bmatrix} + T_X = [T_0 \quad T_1 \quad T_2] \quad (3)$$

Subscripts 0, 1, and 2 represent the Delco thermal test die PST-2, PST-4, and PST-6 respectively. The Q vector represents the power dissipated by each of the die. The b value is the non-linear matrix multiplier and will be further described later. The R-matrix represents the Theta or Psi values and accounts for the thermal cross talk between the die. The T_X value is the reference temperature and the T vector is the resulting die junction temperatures. When describing the R-matrix values in Equation (3), R_{00} is the temperature rise per Watt of power at junction 0 (i.e. the PST-2 die) due to the power dissipated at junction 0. R_{01} is the temperature rise per Watt of power at junction 0 due to the power dissipated at junction 1 (i.e. the PST-4 die), etc. The Theta and Psi values that make up the R-matrix can be obtained from thermal test numbers 1 through 3 as shown in Tables 1 and 2.

Both thermal radiation and natural convection introduce non-linearities that are in accord with known heat transfer physics. In general, Theta and Psi values decrease as power increases in a natural convection environment due to enhanced convection and radiation heat transfer that occurs because of higher surface temperatures. The magnitude of this decrease will vary depending on what is being measured, the size of the die, the size of the package, material properties, etc. As long as the total power level dissipated by the package during normal operation approaches the total power level used to generate the R-matrix of the linear superposition equation (i.e. 2.50W), the die junction temperatures using linear superposition theory will be reasonable. Thus, to improve the accuracy of Equation (3) over a range of total package powers, a non-linear matrix multiplier value b was generated to de-rate the R-matrix accordingly. Thermal test numbers 4 through 8 in Tables 1 and 2 were conducted to obtain non-linear matrix multiplier values that correspond to the Theta and Psi R-matrices. As an example, we will demonstrate the non-linear matrix multiplier value calculation for the Theta JA R-matrix.

Although many elaborate methods can be proposed to create a non-linear matrix multiplier, for the purposes of

Table 3. Theta JA Test Data Used to Obtain Non-Linear Matrix Multiplier

Test	Power (W)					Theta JA (°C/W)						Linear Fit	
No.	PST2	PST4	PST6	Q_{Totl}	$\ln(Q_{Totl})$	PST2	PST4	PST6	R_{Avg}	R_{Stdev}	$\ln(R_{Avg})$	n	a
4	0.25	0.25	0.25	0.75	-0.29	29.7	29.7	27.5	29.0	1.2	3.37	-0.0499	3.3426
5	0.50	0.50	0.50	1.50	0.41	28.7	27.9	25.4	27.3	1.8	3.31		
6	0.75	0.75	0.75	2.25	0.81	28.7	27.5	24.9	27.0	2.0	3.30		
7	1.00	1.00	1.00	3.00	1.10	28.7	27.4	24.5	26.9	2.1	3.29		
8	1.25	1.25	1.25	3.75	1.32	28.6	27.2	24.3	26.7	2.2	3.28		

Table 4. Thermal Conductivity Material Properties.

Material	k (W/m/°C)	Material	k (W/m/°C)
Ball	50.6	Wire	328
Die	87	Conductive Bond	1.5
Substrate Core	0.33	Non-Conductive Bond	0.3
Substrate Mask	0.2	Test PCB Core	0.18
Conductor Traces	393	Test PCB Mask	0.2
Overmold	0.88		

this paper we will use a power law approach. The power law is defined by Equation (4)

$$R_{Avg} = a \cdot Q_{Totl}^{\ n} \qquad (4)$$

For our purposes, we need only to solve for the exponent n. By arranging Equation (4) into the form shown in Equation (5) we can perform a linear least squares curve fit of the power law equation using data from thermal test numbers 4 through 8 to obtain n, which is the resulting slope of the fit.

$$\ln(R_{Avg}) = n \cdot \ln(Q_{Totl}) + \ln(a) \qquad (5)$$

As an example, Table 3 shows the $\ln(R_{Avg})$ and $\ln(Q_{Totl})$ values obtained from Theta JA thermal tests 4 through 8. The resulting slope n was calculated as -0.0499. The non-linear matrix multiplier value b for Equation (3) can now be calculated using Equation (6).

$$b = \left(\frac{\sum_{i=0}^{2} Q_i}{Q_{ref}} \right)^{n} \qquad (6)$$

The numerator of Equation (6) is the sum of the powers for the three stacked die encompassed in the package, Q_{ref} is the power dissipation used to generate the original R-matrix (i.e. 2.50W) and the exponent is the resulting slope of the linear least squares fit of the power law equation (i.e. -0.0499). The resulting linear superposition equation that can be used to estimate die junction temperatures for varying power configurations using Theta JA R-matrix data is shown in Equation (7).

$$[Q_0 \quad Q_1 \quad Q_2] \cdot b \cdot \begin{bmatrix} 35.9 & 30.5 & 24.9 \\ 28.3 & 29.1 & 25.5 \\ 22.3 & 23.0 & 23.7 \end{bmatrix} + T_A = [T_0 \quad T_1 \quad T_2] \qquad (7)$$

Where: $b = \left(\frac{\sum_{i=0}^{2} Q_i}{2.50} \right)^{-0.0499}$ and T_A = Ambient Temp.

Similar equations can be generated using Psi JT, Psi JB, Theta JC and Theta JB data as provided in Tables 1 and 2.

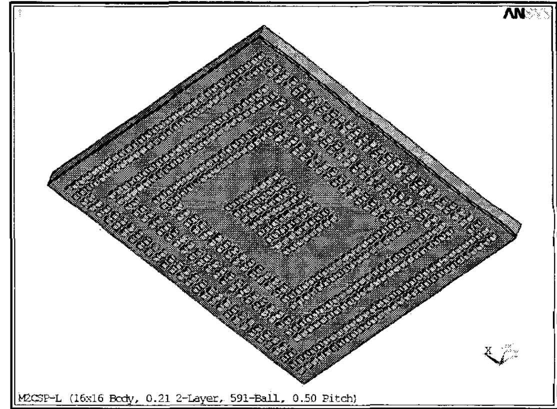

Fig. 4. Finite element model with test PCB structure removed.

It is suggested that multi-die thermal test data is better presented in the form of linear superposition matrix equations that account for the thermal cross talk between die thus allowing users to more accurately calculate multi-die junction temperatures as a function of multi-die power configurations. It has been observed in same die size stacked packages, such as memory devices, that the die tend to stabilize at like temperatures thus facilitating the use of lumped Theta and Psi values due to the close thermal coupling across die even though the individual die powers may vary. However, as highlighted in this study, when stacked die are not of equivalent size,

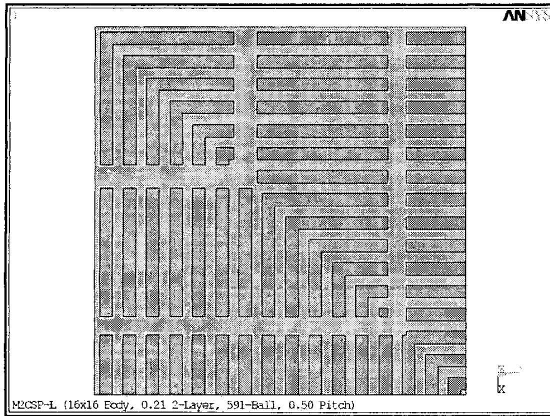

Fig. 5. Simplifed trace pattern (top substrate metal layer).

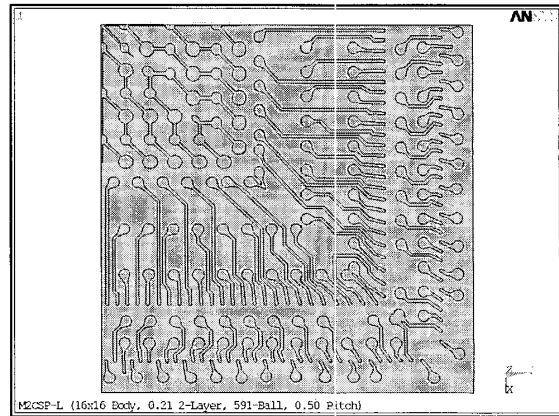

Fig. 6. Complex trace pattern (top substrate metal layer).

Table 5. Theta JA Simulation Data and Test Correlation Error

Test	Simplified Trace Pattern Model						Complex Trace Pattern Model					
	Theta JA Sim (°C/W)			Theta JA Error (%)			Theta JA Sim (°C/W)			Theta JA Error (%)		
No.	PST2	PST4	PST6	PST2	PST4	PST6	PST2	PST4	PST6	PST2	PST4	PST6
1	35.4	29.0	25.6	-1.5	-4.9	+2.9	37.4	31.1	27.8	+4.1	+2.1	+10.5
2	25.4	25.7	23.8	-11.4	-13.0	-7.1	27.4	27.8	25.9	-3.1	-4.7	+1.6
3	19.4	19.5	19.7	-15.3	-18.0	-20.2	21.2	21.4	21.6	-5.4	-7.8	-9.9
4	27.3	25.4	23.6	-8.6	-17.2	-16.5	29.3	27.4	25.7	-1.2	-8.6	-7.1
5	27.6	25.0	23.2	-4.1	-11.7	-9.1	28.9	27.0	25.3	+0.6	-3.4	-0.2
6	26.7	24.7	23.0	-7.6	-11.4	-8.0	28.7	26.7	25.1	-0.2	-3.1	+0.8
7	26.5	24.5	22.8	-8.4	-11.6	-7.6	28.5	26.5	24.9	-0.9	-3.3	+1.2
8	26.3	24.4	22.7	-8.5	-11.6	-7.0	28.3	26.3	24.7	-1.0	-3.2	+1.8

temperature variations across die at varying individual die powers are great enough to require more elaborate presentation, such as in the form of linear superposition matrix equations.

5. Finite Element Models

A commercially available finite element analysis software tool (ANSYS) was applied for thermal simulation purposes. The finite element models were complex enough to include signal traces on both the package substrate and test PCB, individual solder balls, substrate vias interconnecting the substrate metal layers, and die to substrate wire bond connections. Figure 4 displays the model used in the study with the PCB structure removed. All three-dimensional finite element model structures utilized ANSYS SOLID70 elements and a mapped mesh. Interconnect vias and wire bonds were modeled using LINK33 two-dimensional thermal conduction elements. In those models that included detailed metal layer trace routing, the metal traces utilized two-dimensional PLANE55 elements and a free mesh. The freely meshed two-dimensional substrate metal traces were connected to the mapped mesh of the substrate core using ANSYS constraint equations (the reader is referred to the ANSYS CEINTF command). Three-dimensional steady-state laminar flow was assumed for a natural convection environment. This assumption was reflected by the utilization of temperature dependent dual surface isoflux heat transfer coefficients that also assumed laminar flow and accounted for both convection and radiation heat transfer. The derivation and application of these heat transfer coefficients has been previously published by Zahn and Stout [12] and Zahn et al. [13]. Due to the non-symmetric nature of the problem, a full symmtry finite element model was required. The thermal conductivity (k) material properties used in the simulations are shown in Table 4.

Two finite element models were generated and the results evaluated against the previously discussed test data. The first model utilized a top and bottom metal layer simplified trace pattern that facilitated ease of model generation. This type of modeling methodology would be incorporated in order to pro-actively evaluate thermal performance prior to completion of a substrate design. The second model replaced the simplifed metal layer trace patterns with the complex patterns as they exist in the finalized substrate design. Figures 5 and 6 display one-quarter symmetry of the simplified and complex finite element model trace patterns for the top metal layer of the package substrate. The complex trace patterns were created in ANSYS by exporting a SAT file of each

metal layer from the package substrate design tool (Cadence Advanced Package Designer) and importing into ANSYS using the SAT import file option.

Tables 5 displays simulated Theta JA data for thermal test power configurations 1 through 8 as shown in Table 1 along with correlation errors to test data for both the simplifed and complex trace pattern models. The simplified trace pattern model had a greater tendancy to underpredict tested temperatures than the complex trace pattern model. The overall correlation error average for the simplifed trace pattern model was -9.9% compared to -1.7% for the complex trace pattern model. In the case of the test number 3 simulation, the simplified trace pattern model underpredicted die Theta JA values by 15-20% compared to 5-10% for the complex trace pattern model. Industry acceptable errors for package level thermal models can be realistically stated as ±10%, which is exceeded by all of the simplified trace pattern model simulations except for those of test number 1.

All of the testing shown in Tables 1 and 2 (i.e. Theta JA, Psi JT, Psi JB, Theta JC, and Theta JB) were simulated using both the simplified and complex trace pattern finite element models. Results indicated similar correlation trends as was observed with the Theta JA data presented in Table 5. The simplified trace pattern model consistently underpredicted steady-state thermal performance for each of the three stacked die.

The complex trace pattern model provides a level of test verification. Furthermore, it highlights issues that can occur when trying to assess package thermal performance using simplifed trace patterns or by "smearing" substrate metal layer thermal conductivity material properties in an attempt to account for trace routing. Obviously, if the package substrate design has not been finalized it is difficult to pro-actively simulate thermal performance while accounting for complex metal trace routing patterns. However, these results suggest that once a substrate design has been finalized, the "pro-active" thermal simulation analysis needs to be followed by a "verification" analysis that incorporates the details of the physical trace patterns into the model. The descrepancy between the simplifed and complex trace pattern models would have been even greater if not for the large bottom die (10x.16x10.16mm PST-6) which acted to spread the heat over a majority of the substrate surface prior to it reaching the top metal trace layer. As a result of this and other similar studies, a methodology is being developed that will facilitate ease of transfer of complex metal layer trace patterns from the package substrate design layout software (i.e. Cadence Advanced Package Designer) into the thermal finite element modeling software (i.e. ANSYS).

6. Conclusions

Thermal performance testing and finite elment simulations were performed on a 16x16mm, 2-metal layer, 591-ball, 0.50mm pitch, 1.20mm overall height CSP containing an offset pyramid configuration of three stacked Delco thermal test die. Die sizes from bottom-to-top were 10.16x10.16mm (Delco PST-6), 6.35x6.35mm (Delco PST-4), and 3.81x3.81mm (Delco PST-2). Testing and simulations were performed using eight different multi-die power configurations in a natural convection environment to highlight the effects of radiant and convective heat transfer along with thermal cross talk between die.

The thermal performance of multi-die packages, whether the die are configured side-by-side, stacked on top of each other, or a combination of both, cannot be accurately described using the traditional Theta and Psi constants as defined by Equations (1) and (2). As one possible alternative, this study presented a methodology whereby linear superposition theory can be applied. The addition of a non-linear matrix multiplier to the superposition equation allows for greater calculation accuracy over a range of multi-die power configurations by correcting for radiation and convection induced non-linearities.

Furthermore, when pro-actively attempting to simulate thermal performance of laminate based substrate packages, one must be aware that the layout of the signal conductor routing traces has a notable influence on the latteral spreading of heat, and thus the thermal performance of the package. This study provided an example whereby two models were generated using simplified and complex trace patterns. Simulation results indicated that the simplified trace pattern model consistently underpredicted temperatures, whereas the complex trace pattern model provided greater accuracy. It was pointed out that had the bottom die of the three-die stack configuration been smaller, the underprediction of temperatures generated by the simplified trace pattern model would have been greater because the heat would not have been as well spread over the package surface prior to reaching the top metal layer of the laminate substrate.

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