

Copper Core Solder Columns for AI Chip Packages

Remove Heat more Efficiently than Solder Balls

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ABSTRACT

Copper-core solder columns replace traditional BGA solder balls with a cylindrically shaped composite structure consisting of a copper core and a malleable solder sleeve reinforced with a woven architecture of sixteen fine copper-alloy wire filaments. Beryllium copper Be-Cu (C17200) core provides spring-like compliance that limits deformation under mechanical stress, vibration, shock, and extreme thermal conditions ranging from elevated operating temperatures to cryogenic environments.

Thousands of columns can be mounted in an array on large-form-factor (LFF) semiconductor packages used in high-power computing (HPC) AI data-center racks, switches, aerospace, and other harsh-environment applications. Their high thermal conductivity enables more heat transport from the underside of semiconductor devices than solder balls, while their compliant structure absorbs strain caused by coefficient-of-thermal-expansion (CTE) mismatch between large substrates and the PCB, an increasingly important consideration for emerging glass-substrate architectures.

Industry demand for high-performance devices suitable for AI systems, and space-based platforms is accelerating the shift toward larger package sizes with greater thermal and mechanical loads. Copper-core solder columns provide a vertical conduction path from chip undersides toward radiators or warm box structures, and their calculated thermal-conductance values illustrate how they may contribute to system-level heat-management strategies

Indium-based solder coatings and C17200 Be-Cu exhibit material properties that are expected to remain ductile at deep-cryogenic temperatures, including liquid-helium conditions. These characteristics suggest potential applicability in certain quantum-computing environments, although full interconnect-level reliability testing at such temperatures remains future work and is necessary to confirm long-term behavior.

As package dimensions continue to scale, large-form-factor BGA devices face increased risks of warpage, thermal-mechanical fatigue, and signal-integrity degradation. Composite copper-core solder columns offer a combination of mechanical compliance and conductive cross-section that may help address some of these design challenges. Their use is proposed for applications with severe CTE mismatch or

high thermal-mechanical loading. Board-level reliability and drop-in compatibility depend on specific package configurations and require application-specific validation.

Key words: Large Form Factor, LFF, BGA, Solder Column, Cryogenic, Quantum, Glass Core Substrates.

INTRODUCTION

Ball Grid Array (BGA) packaging overtook Column Grid Array (CGA) solutions decades ago due to cost advantages and manufacturing simplicity^{1,2}. Historically, BGA packages were modest in size, typically below 52.5mm. Today, driven by high-power computing (HPC), AI accelerators, and advanced switching fabrics, BGA packages routinely exceed 70mm and are rapidly approaching 180 mm and beyond³.

As package dimensions scale, traditional solder balls encounter increasing thermal-mechanical challenges. Large form-factor (LFF) packages experience substantial coefficient-of-thermal-expansion (CTE) mismatch between the chip substrate and the PCB, resulting in elevated strain energy during thermal cycling^{4,5}. Solder spheres offer limited mechanical compliance which may contribute to cracking, fatigue, and warpage-related issues in certain applications.⁶ This paper focuses on the materials, properties, calculated thermal-conductance behavior, available geometries, and implementation considerations of copper-core solder columns⁷ as an alternative interconnect for large packages.

Solder columns are constructed from three Commercial-Off-The-Shelf (COTS) materials: a center core, a woven sleeve of sixteen fine copper-alloy filaments, and a malleable solder coating that binds the assembly. Solder-coating alloys are selected according to operating temperature and application requirements, including indium-based alloys for cryogenic environments, lead-bearing alloys for aerospace and defense, and lead-free alloys for commercial and AI data-center applications.

Column materials are tailored to application requirements. Lead-free variants for commercial and quantum-related environments are shown in Table 1, while lead-bearing alloys for aerospace, defense, and downhole applications are shown in Table 2.

Table 1. Lead-Free Solder Coating Options

Alloy	Composition	Application
Sn/Ag/Cu (SAC305)	Sn96.5 / Ag3.5 / Cu0.5	AI Data-centers
Sn/Ag/Bi/In	Sn90 / Ag3.5 / Bi0.5 / In6.0	Reduced Temp (Still Above LTS)
Sn/Sb	Sn91.5 / Sb8.5	Automotive
Indium	In99.99	Cryogenic Environments
Indium-Silver	In97 / Ag3.0	Quantum Computers

Table 2. Lead-Bearing Solder Coating Options

Alloy	Composition	Application
Eutectic	Sn63 / Pb37	Aerospace & Defense
Lead-Tin	Pb80 / Sn20 Pb90 / Sn10	Elevated Temp Space & Defense
HMP	Pb93.5 / Sn5 / Ag1.5	High Melting Point Downhole
Indium-Lead	In70 / Pb30 In50 / Pb50	Cryogenic Lunar Surface

The selection of solder coating is governed by the alloy's liquidus temperature, required ductility, and the operating-temperature conditions of the target application. Table 3 summarizes alloys commonly used in cryogenic, commercial, automotive, aerospace, defense and downhole environments including their liquidus temperatures and typical operating ranges. The solder paste used to form the fillets that secure each column to the chip substrate and the PCB after reflow does not need to match the column-coating alloy. The choice of paste alloy is determined by the assembly and process requirements rather than by the material itself.

Table 3. Liquidus Temperature of Solder Coating

Solder Coating	Application Environment	Liquidus Temp	Operating Temp
Indium-Silver In97 / Ag3	Cryogenic Lunar Surface	143°C	-233°C to +125°C
Indium-Lead In70 / Pb30	Cryogenic Lunar Surface	175°C	-273°C to +125°C
Eutectic Sn63 / Pb37	Space & Defense	183°C	-55°C to +125°C
Indium-Lead In50 / Pb50	Space & Defense	210°C	-150°C to +180°C
Sn-Ag-Bi-In	Data Centers HPC	210°C	-55°C to +150°C
SAC305 Sn96.5 / Ag3.5 / Cu0.5	Standard Commercial	218°C	-40°C to +125 °C
Tin-Antimony Sn91.5 / Sb8.5	Automotive & Industrial	243°C	-55°C to +150°C
HMP High-Melting Point Solder	High-Temp Downhole	301°C	-55°C to +275°C

Adjusting the core, sleeve, and coating materials allows column assemblies to be tailored for the specific demands of commercial, AI data-centers, aerospace, defense, cryogenic, and high-temperature systems. These combinations enable optimization of mechanical compliance, thermal conduction, and long-term reliability across a wide range of operating conditions. Table 4 presents six representative material configurations for the core and woven sleeve.

Table 4. Column Core and Woven Sleeve Material Options

Option	Column Core Material	Woven Sleeve	Behavior Characteristics
1	Alloy C17200 Be-Cu	Alloy C17200 Be-Cu	Highest tensile strength. Best springiness for high stress CTE environments.
2		Pd Coated Copper PCC	Good tensile strength. High thermal conductivity. Moderate stress environs.
3	Pd Coated Copper PCC	Alloy C17200 Be-Cu	Moderate tensile strength. Good thermal conductivity. Good CTE compliancy.
4		Pd Coated Copper PCC	Good tensile strength. High thermal conductivity. Moderate compliancy.
5	Pure Copper 99.99%	Alloy C17200 Be-Cu	Moderate tensile strength. High thermal conductivity. Good CTE compliancy.
6		Pd Coated Copper PCC	Good tensile strength. Very high thermal conductivity. Good compliancy.

Composite columns, shown in Figure 1 are constructed by combining three materials: a center core, a woven sleeve consisting of sixteen fine copper-alloy filaments that surround the core, and a malleable solder coating that mechanically secures the assembly. Copper options include C17200 (Be-Cu), palladium coated copper (PCC) or pure copper, selected according to the mechanical and thermal requirements of the target application.

**Figure 1.** (a) Solder Columns shown prior to solder coating. (b) The same column is shown after solder coating and mounting on a pad with a solder fillet.

COLUMN LENGTH: LONG VS. SHORT

Column length balances mechanical compliance and thermal performance. Experimental studies have shown that taller columns exhibit significantly higher fatigue lifetime⁷. Longer columns flex more and are expected to reduce strain energy under severe CTE mismatch, while shorter columns increase stiffness and reduce thermal resistance. These behaviors follow established mechanical and thermal principles, although reliability outcomes depend on specific package configurations and require further validation.

A practical guideline is to use smaller-diameter columns or to increase column length to enhance mechanical compliance and reduce strain energy during thermal cycling. Length-to-diameter (L/D) ratios above 4:1 allow the column to flex more effectively, which is expected to reduce localized strain at the solder-to-pad interface. When CTE mismatch is less critical, shorter columns (L/D < 3:1) may be selected to increase stiffness, reduce package height, improve electrical performance, or satisfy system-level mechanical or thermal constraints. These recommendations reflect general mechanical behavior rather than demonstrated reliability results for specific package designs.

Columns offer a tunable interconnect structure that combines mechanical compliance with conductive cross-section for heat transport. These characteristics make column architectures a candidate for large semiconductor packages where traditional solder balls may encounter elevated thermal-mechanical stresses. Table 5 illustrates representative length-to-diameter combinations. The suitability of any specific geometry for package-level reliability depends on full assembly design and requires application-specific validation.

Table 5. Examples of Column Length-to-Diameter Ratios

Column Diameter	Solder Column Length		
	3:1	4:1	6:1
0.125 mm	0.38 mm	0.50 mm	0.75 mm
0.150 mm	0.45 mm	0.60 mm	0.90 mm
0.200 mm	0.60 mm	0.80 mm	1.20 mm
0.230 mm	0.69 mm	0.92 mm	1.38 mm
0.250 mm	0.75 mm	1.00 mm	1.50 mm
0.300 mm	0.90 mm	1.20 mm	1.80 mm
0.330 mm	0.99 mm	1.32 mm	1.92 mm
0.380 mm	1.14 mm	1.52 mm	2.28 mm
0.400 mm	1.20 mm	1.60 mm	2.40 mm
0.450 mm	1.35 mm	1.80 mm	2.70 mm
0.500 mm	1.50 mm	2.00 mm	3.00 mm

COLUMN DIAMETER TO PAD DIAMETER RATIO

The column diameter is constrained by the solderable pad diameter on both the package substrate and the PCB. In many designs, the package substrate was originally configured for solder balls, requiring package designers to retro-fit an appropriate column diameter to the existing pad geometry.

Unlike solder balls, columns must be smaller than the pad diameter on both the chip package and the PCB to allow formation of a properly shaped solder fillet during reflow. This fillet establishes a stable solder joint between the column and the pad. The smaller of the package-pad or PCB-pad diameters determines the maximum allowable column diameter to ensure sufficient solder volume in the surrounding fillet.

Table 6 provides design guidelines for selecting column diameters based on pad size. Determining the optimal pad-to-column ratio is not exact, but practical fillet-formation rules apply: the solder fillet should not wick up more than one-third of the column height at either end.

Table 6. Pad Diameter Drives the Column Diameter

Column Diameter	Max Diameter of Package Pad	Ratio Pad Diameter to Column Diameter
0.125 mm	0.200 mm	1.60 : 1
0.150 mm	0.250 mm	1.66 : 1
0.200 mm	0.320 mm	1.60 : 1
0.230 mm	0.360 mm	1.60 : 1
0.250 mm	0.400 mm	1.60 : 1
0.300 mm	0.450 mm	1.60 : 1
0.330 mm	0.530 mm	1.60 : 1
0.380 mm	0.610 mm	1.60 : 1
0.400 mm	0.640 mm	1.60 : 1
0.450 mm	0.720 mm	1.60 : 1
0.500 mm	0.800 mm	1.60 : 1

Typically, the package pad and PCB pad must be larger than the diameter of the solder column as show in Figure 2.

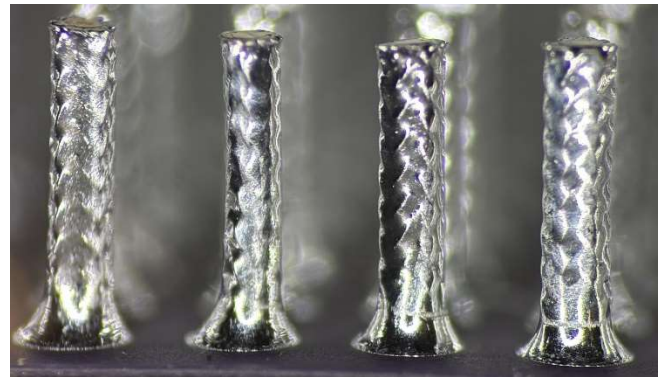


Figure 2. Copper-core Solder Columns mounted on a substrate pad with a frustum shaped solder fillet.

SOLDER PASTE STENCIL GEOMETRIES

Columns are attached and reflowed to package pads using a controlled volume of solder. The volume of solder contained in the frustum-shaped fillet around each column can be adjusted by selecting paste-stencil apertures and foil thicknesses, as shown in Table 7. Stencil apertures are typically 30 to 90 μm (1.5 to 2.3 mils) smaller than the pad diameter to help avoid excessive solder deposition, which can

lead to bridging during reflow, or insufficient deposition, which can limit fillet formation.

Stencil foil thickness also influences solder volume. Thicker foils deposit more paste and are generally used for larger pad diameters or in situations where additional fillet volume may be desirable. Thinner foils improve release characteristics for small apertures and help reduce over-printing on fine-pitch pads. In practice, designers often evaluate multiple stencils with incrementally varied apertures and foil thicknesses to identify geometries suitable for a given pad configuration.

Table 7. Pad Diameter Drives the Stencil Geometries

Package Pad Diameter	Column Diameter	Stencil Foil Thickness	Aperture Solder Paste Stencil
0.200 mm	0.125 mm	0.075 mm	0.12 ~ 0.17 mm
0.250 mm	0.150 mm	0.100 mm	0.17 ~ 0.22 mm
0.320 mm	0.200 mm	0.125 mm	0.23 ~ 0.28 mm
0.400 mm	0.250 mm	0.125 mm	0.30 ~ 0.36 mm
0.450 mm	0.300 mm	0.150 mm	0.36 ~ 0.41 mm
0.640 mm	0.400 mm	0.150 mm	0.52 ~ 0.60 mm
0.700 mm	0.450 mm	0.200 mm	0.61 ~ 0.66 mm
0.750 mm	0.500 mm	0.200 mm	0.66 ~ 0.71 mm

STRESS ABSORPTION - CTE MISMATCH

Table 8 summarizes the coefficient of thermal expansion (CTE) for common substrate and PCB materials. The length-to-diameter (L/D) ratio of columns, combined with intentional material selection, provides a mechanically compliant interconnect structure that can flex under thermal-mechanical loading. This behavior is relevant for applications with severe CTE mismatch, including emerging glass-core substrates.

Large temperature excursions drive repeated expansion and contraction of both the package and the PCB. When a device has a large distance-from-neutral point (DNP), the outermost interconnects experience higher shear displacement because the package corners travel farther than the center during thermal cycling. In general, interconnects at high-DNP locations are subject to greater fatigue stresses. Cyclic strain can initiate micro-cracks at the solder-to-pad interface, which may propagate under continued thermal cycling. In large-format packages, the combination of high DNP, CTE mismatch, and aggressive thermal environments is often discussed in the literature as contributing to solder-joint fatigue mechanisms, illustrated conceptually in Figure 3.

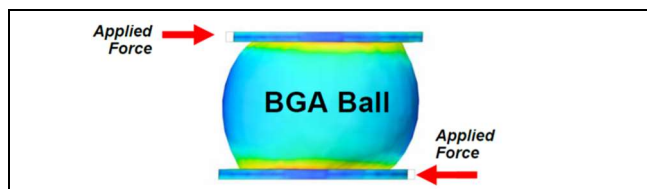


Figure 3. FEA: Stress on Solder Ball Causing Fractures

Table 8. CTE of Various Substrate Materials

Material	Application Purpose	CTE Coefficient of Thermal Expansion
Fused Silica	High Temp Optics	0.55 ppm/°C
Silicon	Wafers/Die	2.7 ppm/°C
Glass	Package Substrate	3.3~5.0 ppm/°C
Ceramic Al ₂ O ₃	Package Substrate	6.7 ppm/°C
BT Resin	BGA Substrate	10 ppm/°C
Build-up Film	FC-BGA & HPC Substrates	14~22 ppm/°C
FR4	Main PCB	17 ppm/°C

SELECTING COLUMN MATERIALS ACCORDING TO USES AND APPLICATION

Table 9 summarizes representative material combinations for fabricating columns intended for specific applications and operating environments. The core, woven sleeve, and solder-coating alloys are selected to provide appropriate mechanical compliance and thermal behavior for each use case, with long-term reliability dependent on application-specific validation and test conditions.

Table 9. Column Material Options by Application

Target Application	Core Material	Woven Sleeve	Solder Coating Options
Cryogenic and Quantum	C17200 (Be-Cu)	C17200 (Be-Cu)	In97 Ag3
Space & Defense	C17200 (Be-Cu)	C17200 (Be-Cu) or Palladium Coated Copper (PCC)	Sn63 Pb37 Pb80 Sn20 Pb 90 Sn10
Data Centers in Space			In97 Ag3 In50 Pb50 In70 Pb30
Land Based Data Centers			Sn Ag3.0 Bi0.5 In6.0 or SAC305
Automotive			Sn91.5 Sb8.5
Downhole			HMP Pb93.5 Sn5 Ag1.5

SELECTING COLUMN MATERIALS ACCORDING TO USES AND APPLICATION

Table 9 summarizes representative material combinations for fabricating columns intended for specific applications and operating environments. The core, woven sleeve, and solder-coating alloys are selected to provide appropriate mechanical compliance and thermal behavior for each use case, with long-term reliability dependent on application-specific validation and test conditions.

Table 10. Thermal Conductivity of Materials in Columns.

Material	Composition	Thermal Conductivity
C17200 (Alloy 25) Beryllium-Copper	Cu98/Be1.8/Co0.2	105 W/(m·K)
PCC Palladium Coated Copper	99.99% Cu with thin Pd coating	380 W/(m·K)
Pure Copper	99.99% Cu	400 W/(m·K)

COLUMN CORE GEOMETRIES AND THERMAL CONDUCTANCE

The column's copper core is fully enclosed by a woven sleeve consisting of sixteen small-diameter copper filaments. The core and sleeve are coated with a thin layer of hot, malleable solder that bonds the sleeve to the exterior surface of the core. Through capillary action, molten solder fills and coats the open spaces between the filaments, forming a continuous solder layer around the column assembly.

The overall column diameter is approximately equal to the core diameter plus four times the filament diameter of the woven sleeve as shown in section view in Figure 4. The outside diameter (O.D.) of the column can be adjusted by selecting appropriate combinations of core diameter and sleeve-filament size, as shown in Table 11.

Columns with O.D. diameters of 0.125 mm and 0.15 mm typically use a C17200 copper core surrounded by a woven sleeve of sixteen C17200 filaments. Columns with O.D. diameters of 0.20 mm and larger generally use a C17200 copper core surrounded by a woven sleeve of sixteen palladium-coated copper (PCC) filaments or C17200 filaments. These material selections are based on mechanical and thermal property considerations; they do not represent demonstrated reliability outcomes for specific package configurations, and package-level behavior requires application-specific validation.

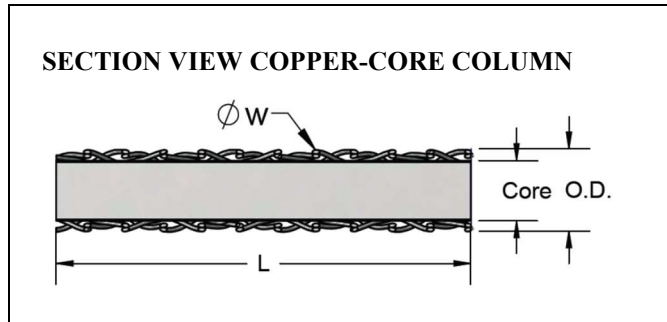


Figure 4. Column O.D. equals the core diameter plus four times the sleeve-filament diameter. Column length (L) is typically 3:1 to 5:1 relative to O.D., selected according to CTE mismatch and heat-transport requirements.

Table 11. Per-Column Thermal Conductance (G) at L=1.0mm, vs. Column Diameter (O.D.) and Core/Sleeve Materials and Geometry.

Column Diameter (O.D.)	Copper Core Diameter	Sleeve Filament Diameter	Per-Column Thermal Conductance (G) Length=1.0 mm
0.125 mm	0.025 mm C17200	0.025 mm C17200	0.00088 W/K
0.150 mm	0.050 mm C17200	0.025 mm C17200	0.00103 W/K
0.200 mm	0.050 mm C17200	0.038 mm PCC	0.00721 W/K
0.230 mm	0.070 mm C17200	0.038 mm PCC	0.00741 W/K
0.250 mm	0.100 mm C17200	0.038 mm PCC	0.00783 W/K
0.300 mm	0.100 mm C17200	0.050 mm PCC	0.01300 W/K
0.330 mm	0.125 mm C17200	0.050 mm PCC	0.01350 W/K
0.380 mm	0.125 mm C17200	0.060 mm PCC	0.01890 W/K
0.400 mm	0.125 mm C17200	0.070 mm PCC	0.02510 W/K
0.450 mm	0.150 mm C17200	0.070 mm PCC	0.02570 W/K
0.500 mm	0.200 mm C17200	0.070 mm PCC	0.02710 W/K

SIGNIFICANCE OF THERMAL CONDUCTANCE

Thermal conductance describes how effectively a column can transfer heat along its length for a given temperature difference. Conductance depends on both the thermal conductivity of the materials and the combined cross-sectional area of the copper core and the sixteen filaments in the woven sleeve. Columns with larger core diameters or thicker sleeve filaments exhibit higher calculated conductance values. These per-column conductance values are used to model array-level heat-movement behavior, since the conductance of many columns operating in parallel can be summed to represent a potential thermal-transport pathway between the package and the PCB. Table 12 evaluates these modeled array-level heat-movement estimates for multiple package sizes and column lengths; actual system-level thermal performance depends on complete thermal-stack design and requires application-specific validation.

HEAT MOVEMENT – DATA CENTERS IN SPACE

Copper-core solder column arrays provide a potential thermal-transport pathway for space-based data-center architectures, where conventional cooling mechanisms are unavailable. In vacuum, processors and power modules cannot transfer heat through convection, and conduction paths are limited to the structural interfaces designed into the system. Column arrays form a dense network of mechanically compliant, high-conductivity elements that may contribute to

heat transfer from the underside of the device package into the underlying board and chassis, where radiators dissipate it by radiation.

Because each column acts as an independent conduction element, the array's calculated heat-transport capacity scales with pin count. This behavior follows from the thermal-conductance values presented earlier and reflects the additive nature of parallel conduction paths. These principles suggest that column arrays may help moderate thermal gradients in large packages operating in orbital or lunar environments, although system-level thermal performance depends on specific package designs and requires application-specific validation.

HEAT MOVEMENT-LAND BASED DATA CENTERS

High-performance computing (HPC) data centers increasingly operate at power densities that challenge traditional package-to-board interconnects, making conduction-based heat removal an important design consideration. Copper-core solder column arrays provide a mechanically compliant, high-conductivity interface that can transfer heat from processors, accelerators, and memory modules into cold-plate, liquid, or immersion-cooling infrastructure. Unlike rigid interconnects, columns maintain structural continuity under thermal cycling and offer many parallel conduction paths whose calculated heat-transport capacity scales with pin count.

These calculated conductance values indicate that column arrays may help moderate hotspot formation and improve thermal distribution across large substrates, although the extent of any system-level thermal benefit depends on the complete cooling architecture and requires application-specific validation.

THERMAL-CONDUCTANCE RATIONALE AND COLUMN DESIGN CONSIDERATIONS

Composite solder-column interconnects may be a consideration in systems where thermal transport and mechanical compliance are important design constraints. Solder balls provide minimal conductive cross-section and are not intended to serve as heat-transfer elements. Their thermal contribution is typically negligible at power densities associated with modern HPC and accelerator-class devices. In contrast, each composite column functions as an independent conduction pathway whose calculated thermal conductance supports modeled watt-level heat movement from the device package toward the system-level cooling infrastructure. When deployed in large arrays, the additive nature of these conduction paths represents a scalable network whose modeled behavior suggests potential reductions in temperature gradients across the substrate. Any system-level effects, such as cooling-power implications, reliability outcomes, or sustained power capability, depend on the complete thermal architecture and require application-specific validation. Column adoption therefore reflects

interest in interconnect structures that combine mechanical compliance with conductive cross-section, with total cost and performance determined at the system level for each application.

The relevance of column-based interconnects becomes apparent when considering the thermal-mechanical environment of high-power compute modules. Localized temperature excursions and rapid thermal cycling are known to correlate with thermal throttling, accelerated aging, and interconnect fatigue in large packages. Column arrays provide many parallel conduction paths, and their calculated thermal-conductance values suggest that they may help moderate temperature gradients by distributing heat more uniformly across the package footprint. Potential system-level effects such as reduced cooling demand or improved power stability depend on the complete thermal architecture of the device and require application-specific modeling or measurement to validate. From a design-perspective, column adoption reflects an interest in interconnect structures that combine mechanical compliance with conductive cross-section, although total cost of ownership and reliability outcomes must be evaluated at the system level for each application.

With the per-column thermal-conductance values established in Table 11, the next step is to evaluate how these individual columns behave when thousands of them are arranged into full arrays across different package sizes. To illustrate the magnitude of heat that can be transported through column arrays, Table 12A summarizes the calculated thermal-conduction capacity of copper-core columns at three practical column lengths (1.0 mm, 1.6 mm, and 2.2 mm) for a temperature differential of $\Delta T = 20$ K. Table 12B is organized by column diameters (O.D.) at the same three column lengths. These results show how modeled heat-transport capability varies with column length and pin count, providing a basis for selecting column geometries in high-power applications.

Taken together, Tables 12A and 12B illustrate key thermal-design behaviors. Modeled results indicate that shorter columns and larger diameters yield higher calculated heat-transport values, and total array conductance increases with pin count. The data also highlights a core design tradeoff: geometries that increase calculated heat movement reduce mechanical compliance, which can increase thermomechanical strain at high-DNP locations. Column geometries can therefore be adjusted by selecting appropriate material tensile strengths and composite diameters and lengths, allowing designers to balance mechanical compliance with thermal-conductance objectives. System-level thermal performance, however, depends on the complete package and cooling architecture and requires application-specific validation.

Table 12A. Heat moved in column arrays for $\Delta T = 20$ K
Organized by Column Length

Column Length	Column Diameter (O.D.)	Heat Movement Watts (W) at $\Delta T = 20$ K (Per Package mm)			
		1936 Pins	4201 Pins	9001 Pins	14,400 Pins
		45SQ	70SQ	100SQ	125SQ
0.5mm	0.12mm	68	148	352	506
	0.15mm	252	548	1174	1878
1.0mm	0.20mm	279	606	1298	2076
	0.25mm	303	658	1410	2255
	0.30mm	503	1092	2340	3744
	0.40mm	972	2109	4518	7230
	0.50mm	1049	2277	4879	7810
1.6mm	0.20mm	174	379	811	1297
	0.25mm	190	411	881	1410
	0.30mm	315	683	1463	2340
	0.40mm	607	1318	2824	4520
	0.50mm	656	1423	3049	4880
2.2mm	0.20mm	127	276	591	944
	0.25mm	138	299	641	1025
	0.30mm	299	497	1064	1702
	0.40mm	441	958	2052	3283
	0.50mm	476	1034	2214	3542

Table 12B. Heat moved in column arrays for $\Delta T = 20$ K
Organized by Column Diameter.

Column Diameter (O.D)	Column Length	Heat Movement Watts (W) at $\Delta T = 20$ K (Per Package)			
		1936 Pins	4201 Pins	9001 Pins	14,400 Pins
		45SQ	70SQ	100SQ	125SQ
0.15 mm	0.5mm	252	548	1174	1878
	1.0 mm	126	274	587	939
0.20 mm	0.5mm	558	1212	2596	4152
	1.0 mm	279	606	1298	2076
	1.6 mm	174	379	811	1297
	2.2 mm	127	276	591	944
0.25 mm	0.5mm	606	1316	2820	4510
	1.0 mm	303	658	1410	2255
	1.6 mm	190	411	881	1410
	2.2 mm	138	299	641	1025
0.30mm	1.0 mm	503	1092	2340	3744
	1.6 mm	315	683	1463	2340
	2.2 mm	229	497	1064	1702
0.40mm	1.0 mm	972	2109	4818	7230
	1.6 mm	607	1318	2824	4520
	2.2 mm	441	958	2052	3283
0.50mm	1.0 mm	1049	2277	4879	7810
	1.6 mm	656	1423	3049	4880
	2.2 mm	476	1034	2214	3542

$\Delta T = 20$ K is chosen because it represents a realistic thermal gradient across large packages under high-power operation, providing a meaningful basis for comparing column conductance without exceeding typical junction-to-board temperature differences.

Furthermore, it is best practice to keep part of the column exposed outside the fillet, since fully entombed columns experience higher interface thermal resistance and reduced heat-transfer efficiency, along with increased joint stiffness that elevates thermomechanical strain at high-DNP sites. Maintaining column exposure also preserves a more direct copper-to-pad heat path, which keeps the interface resistance low and allows the column's intrinsic conductance to be fully utilized. In addition, limiting fillet encroachment helps retain the column's designed compliance, reducing the tendency for the joint to behave like a rigid post under package warpage and high-DNP shear loading.

COLUMN PULL STRENGTH TEST

MIL-STD-883K Method 2038 defines a destructive axial-tension test to evaluate the mechanical integrity of a solder column attached to a package. In this method, each column is pulled vertically at a controlled rate of 25.4 mm per minute, without shock loading, until failure occurs. The standard specifies minimum acceptable pull strength of 2,810 grams-force per square millimeter of column cross-sectional area, allowing the required force to be scaled directly from column diameter. Representative diameters and their corresponding minimum pull strengths are listed in Table 13 as tested on the pull-strength tester with video view shown in Figure 5.

During testing, failures consistently fall into three distinct categories, each revealing a different weakness in the interconnect structure:

- (a) Column Failure: Fracture through the column core
- (b) Pad/Column Joint Failure: Separation at the solder-to-pad attachment interface
- (c) Pad Failure: Detachment of the pad from the package substrate

These failure modes provide insight into column metallurgy, joint quality, and substrate robustness, offering mechanical information relevant to second-level reliability considerations.

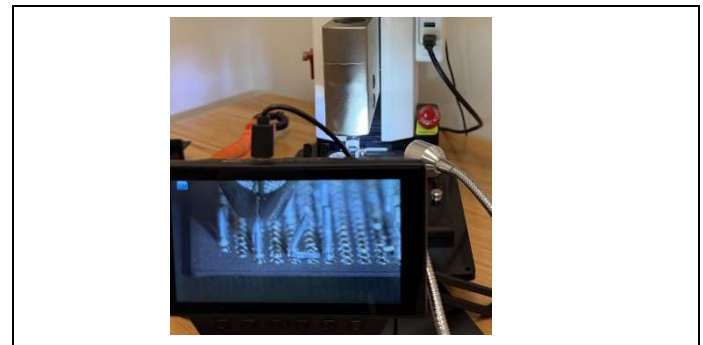


Figure 5. Destructive column pull-strength tester

Table 13. 0.51mm Diameter Column Pull Strength Test

Column Type Under Test (DUT)	MIL-STD-883K Method 2038			
	Cross Sectional Area (mm ²)	Minimum Pull Strength TM2038	Actual Pull Strength	Failure Code
Pb90 Sn10 Plain	0.2028	575 gF	696 gf	(a)
Pb80 Sn20 Copper Wrap	0.2028	575 gF	804 gf	(a)
Pb80 Sn20 Copper Braided	0.2028	575 gF	1020 gf	(a)
Copper Core C172	0.2028	575 gF	>2500gf	(b)

(a) Failure occurs through the column core (b) Occurs at pad/column attach point (c) Pad separates from package.

DC RESISTANCE OF THE COLUMN

The DC resistance of a solder column provides a useful reference for understanding its electrical contribution within the interconnect structure. Table 14A summarizes the resistance per millimeter (mm) of column length for the various diameters used in compliant column assemblies. Resistance was measured by applying a digital ohm-meter across a 200 mm continuous length of column wire prior to cutting the material into individual columns. The measured value was then divided by 200 to obtain the DC resistance per millimeter, as reported in the table.

The copper core, the woven sleeve, and the solder coating act as parallel electrically conductive paths. The total column resistance is the reciprocal of the sum of their individual conductance. As expected, columns with smaller diameters exhibit significantly higher resistance due to reduced cross-sectional area and higher current density within each conductive element. Conversely, larger-diameter columns provide lower resistance and therefore lower resistive (Joule) (I^2R) heating and voltage drop.

Table 14A. DC Resistance at Column Length = 1.0 mm

O.D. Col Dia (mm)	Copper Core Solder Column				DCR mΩ/mm
	Core		16x Mesh Sleeve		
	Mat'l	Dia (mm)	Mat'l	Dia (mm)	
0.125	C172	0.025	C172	0.025	2.10
0.150	C172	0.050	C172	0.025	2.00
0.200	C172	0.050	PCC	0.038	0.91
0.230	C172	0.070	PCC	0.038	0.89
0.250	C172	0.100	PCC	0.038	0.85
0.300	C172	0.100	PCC	0.050	0.51
0.330	C172	0.125	PCC	0.050	0.50
0.380	C172	0.125	PCC	0.060	0.35
0.400	C172	0.125	PCC	0.070	0.26
0.450	C172	0.150	PCC	0.070	0.26
0.500	C172	0.200	PCC	0.070	0.25

Table 14B. DC Resistance at Specific Column Lengths

O.D. Column Diameter (mm)	Copper Core Solder Column Length			
	DCR mΩ 0.5 mm	DCR mΩ 1.0 mm	DCR mΩ 1.6 mm	DCR mΩ 2.2 mm
0.125	1.050	2.10	3.36	4.62
0.150	1.000	2.00	3.20	4.40
0.200	0.455	0.91	1.46	2.00
0.230	0.445	0.89	1.43	1.96
0.250	0.425	0.85	1.36	1.87
0.300	0.255	0.51	0.82	1.12
0.330	0.250	0.50	0.80	1.10
0.380	0.175	0.35	0.56	0.77
0.400	0.130	0.26	0.42	0.57
0.450	0.130	0.26	0.42	0.57
0.500	0.125	0.25	0.70	0.55

These results show that total column resistance is governed by the combined parallel conductance of the copper core and the 16-filament sleeve. Small-diameter columns carry higher resistance, while larger-diameter columns benefit from both increased core area and a more conductive sleeve. This trend directly influences resistive (Joule) heating and voltage drop in dense interconnect arrays, making column diameter and sleeve architecture important electrical-design parameters for high-current, high-reliability applications.

SOLDER BALL VS. COLUMN DIAMETERS

Solder columns are manufactured in a wide range of diameters and alloy systems. Solder columns are significantly smaller in diameter than a corresponding solder ball used on any given pad diameter. Solder columns are cylindrical, and their reduced diameter ensures that, during reflow, a solder fillet can form around the entire circumference of the column, as illustrated earlier in Figure 1(b). A full 360° fillet is preferred for mechanical robustness, though a fillet covering at least 270° is acceptable in some applications. To achieve this, a solder paste stencil is used to deposit a controlled volume of solder paste onto each pad prior to column attachment and reflow as described in Table 7.

Solder balls are geometrically structured differently than columns. Before reflow, BGA spheres diameters are typically 20% larger than solder-mask-defined (SMD) pads, as shown in Figure 6(a). The oversizing of solder balls is intentional: the ball overlaps the pad and collapses during reflow. In contrast, for non-solder-mask-defined (NSMD) pads, the solder ball diameter (before reflow) generally matches the pad diameter, as shown in Figure 6(b). Because the NSMD pad exposes more copper and has no solder mask “collar,” the ball does not require oversizing to achieve proper wetting.

When a solder ball is reflowed onto an SMD package pad but the PCB uses an NSMD via-in-pad structure, the ball collapses cleanly within the package’s mask opening while the molten solder on the PCB side wets uniformly into the via land, typically producing a slightly asymmetric but generally centered joint profile with limited lateral distortion.

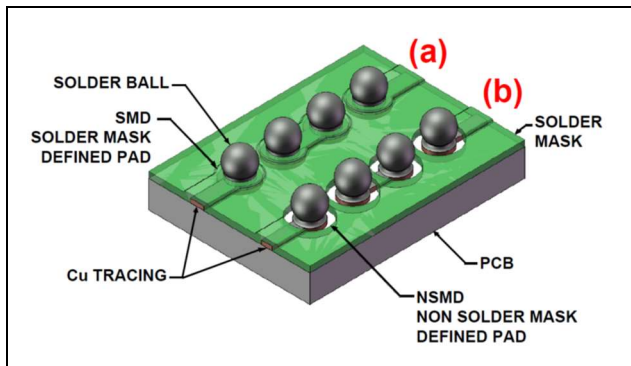


Figure 6. Solder Balls on SMD and NSMD PADS

This geometric distinction is not merely a manufacturing artifact; it is central to the mechanical-design rationale for column-based interconnects. Columns rely on compliant geometry and a robust fillet to manage strain energy, whereas solder balls rely on collapse behavior and volumetric wetting. As package sizes increase and CTE mismatch becomes more severe, these differences become increasingly consequential.

This design relationship is summarized in three bullet points below and is described in more detail in Table 15

- Solder balls are always larger than SMD Pads.
- Balls are roughly same diameter as NSMD Pads.
- Solder columns are always smaller than the pad

Table 15. Solder Ball vs. Solder Column Diameters

Diameter Solder Mask Defined Pad (SMD)	Ball Diameter Before Reflow	Solder Column Diameter (Nom)	Pitch Typical (Ref Only)
0.200 mm	0.250 mm	0.125 mm	0.40 mm
0.250 mm	0.300 mm	0.150 mm	0.50 mm
0.280 mm	0.350 mm	0.175 mm	0.65 mm
0.330 mm	0.400 mm	0.200 mm	0.80 mm
0.360 mm	0.450 mm	0.230 mm	0.80 mm
0.400 mm	0.500 mm	0.250 mm	0.80 mm
0.500 mm	0.635 mm	0.300 mm	1.0 mm
0.610 mm	0.760 mm	0.380 mm	1.27 mm
0.750 mm	Note 1	0.450 mm	1.0mm
0.800 mm	Note 1	0.500 mm	1.0 mm

Note 1: Solder balls not typically used

TENSILE STRENGTH AND MECHANICAL LOAD CAPACITY OF C17200 COPPER-CORE COLUMNS

Tensile values establish the fundamental axial strength of the copper-core column architecture and provide a baseline for understanding how these structures respond to direct mechanical loading. Table 16A and Table 16B summarize the tensile strength and breaking-load performance of columns constructed with a high-strength C17200 beryllium-copper core paired with either a lower-strength C17200 sleeve or a PCC sleeve, bonded by a thin solder coating.

Table 17 presents corresponding data for columns using a 99.99 % copper core with PCC sleeve filaments. The combined mechanical contribution of the core and the multi-filament sleeve produce significant axial load capacity even at small diameters, with breaking loads increasing as total copper cross-section grows. Lower-strength sleeve materials (such as PCC) reduce overall UTS, but the core remains the dominant contributor to axial strength. These tensile values characterize column behavior under axial loading and provide input parameters for evaluating mechanical response in broader package-level analyses.

Columns with higher breaking loads may exhibit greater resistance to buckling and plastic deformation under assembly-related forces, rework stresses, or thermally induced strain. The multi-filament sleeve architecture distributes mechanical load among several copper elements, which may help reduce localized stress concentrations at the solder interface or within the core. Potential implications for thermal-cycle performance depend on the complete package design and require application-specific reliability testing or appropriate modeling to confirm. The tensile metrics presented here therefore serve as material-level inputs for mechanical-design considerations rather than demonstrated indicators of system-level reliability.

Table 16A. UTS Tensile Strength Columns High Strength C17200 Core and Annealed C17200 Sleeve

Column O.D.	Materials		UTS MPa Nom	Breaking Load gF Nom
	Core C17200 Note (1)	Sleeve C17200 Note (2)		
0.125 mm	0.025 mm	0.025 mm	450	558
0.150 mm	0.050 mm	0.025 mm	446	804

Note (1): Tensile Strength 221 KSI (UTS 1500 MPa)

Note (2): Tensile Strength 85 KSI (UTS 590 MPa)

Table 16B. UTS Tensile Strength Columns High Strength C17200 Core and PCC Sleeve

Column O.D.	Materials		UTS MPa Nom	Breaking Load gF Nom
	Core C17200 Note (1)	Sleeve PCC Note (3)		
0.200 mm	0.050 mm	0.038 mm	223	716 gF
0.230 mm	0.070 mm	0.038 mm	253	1027 gF
0.250 mm	0.100 mm	0.038 mm	332	1660 gF
0.300 mm	0.100 mm	0.050 mm	273	1970 gF
0.330 mm	0.125 mm	0.050 mm	316	2670 gF
0.380 mm	0.125 mm	0.060 mm	261	3020 gF
0.400 mm	0.125 mm	0.070 mm	260	3340 gF
0.450 mm	0.150 mm	0.070 mm	263	4270 gF
0.500 mm	0.200 mm	0.070 mm	323	6460 gF

Note (1): Tensile Strength 221 KSI (UTS 1500 MPa)

Note (3): Tensile Strength 31 KSI (UTS 215 MPa)

Table 17. UTS Tensile Strength Columns 99.99 Cu Core

Column O.D.	Materials		UTS MPa Nom	Breaking Load Nom
	Core Pure Cu Note (3)	Sleeve PCC Note (3)		
0.200	0.050 mm	0.038 mm	215	440 gF
0.230	0.070 mm	0.038 mm	215	480 gF
0.250	0.100 mm	0.038 mm	215	570 gF
0.300	0.100 mm	0.050 mm	215	860 gF
0.330	0.125 mm	0.050 mm	215	960 gF
0.380	0.125 mm	0.060 mm	215	1260 gF
0.400	0.125 mm	0.070 mm	215	1620 gF
0.450	0.150 mm	0.070 mm	215	1740 gF
0.500	0.200 mm	0.070 mm	215	2050 gF

Note (3): Tensile Strength 31 KSI or UTS 215 MPa

GLASS-CORE SUBSTRATE INTERCONNECT CONSIDERATIONS

Glass core substrates are rapidly emerging in high density packaging with exceptional dimensional stability, fine line capability, and uniform electrical performance. However, their low CTE, typically 3~5ppm/°C, creates a significant mismatch with the surrounding package materials. Traditional solder balls struggle under these conditions, generating high strain energy, early crack initiation, and shortened fatigue life.

Solder columns provide a more resilient interconnect for glass-core architectures. Their composite structure delivers consistent stand-off height and the mechanical compliance needed to absorb CTE-driven strain, reducing stress concentrations and supporting mechanical behavior relevant to long-term reliability. This mechanical advantage becomes increasingly important as package sizes grow and interconnect counts increase.

Thermally, glass substrates conduct heat poorly in the vertical direction, making efficient heat removal essential. Copper-core columns support modeled watt-level conduction per column and exhibit significantly lower interface thermal resistance compared to solder balls. Modeled behavior indicates potential improvements in temperature uniformity, reduced hot-spot formation, and lower cooling burden for AI accelerators, HPC modules, and other high-power systems adopting glass-core technology.

The dimensional stability of glass also enables tighter pitch and more uniform pad geometries, which align well with the controlled collapse and predictable wetting behavior of solder columns. Columns maintain consistent stand-off height across large arrays, improving co-planarity and reducing warpage-induced stress during assembly. As glass-core substrates scale toward larger panels and higher interconnect densities, copper-core columns may offer mechanical compliance, thermal efficiency, and geometric stability advantageous in scenarios where traditional solder balls face limitations.

SUMMARY

This paper presents an evaluation of copper-core solder columns as an alternative to traditional solder balls for large form factor (LFF) semiconductor packages, represented schematically in Figure 7. Conventional solder balls encounter thermo-mechanical challenges driven by CTE mismatch, warpage, and elevated power densities as package sizes extend beyond 70 mm toward 180 mm and larger. Copper-core columns employ a composite architecture consisting of a high-strength copper core, a malleable solder coating, and a woven sleeve of fine copper filaments, providing a different mechanical and thermal-transport structure than solid solder balls.

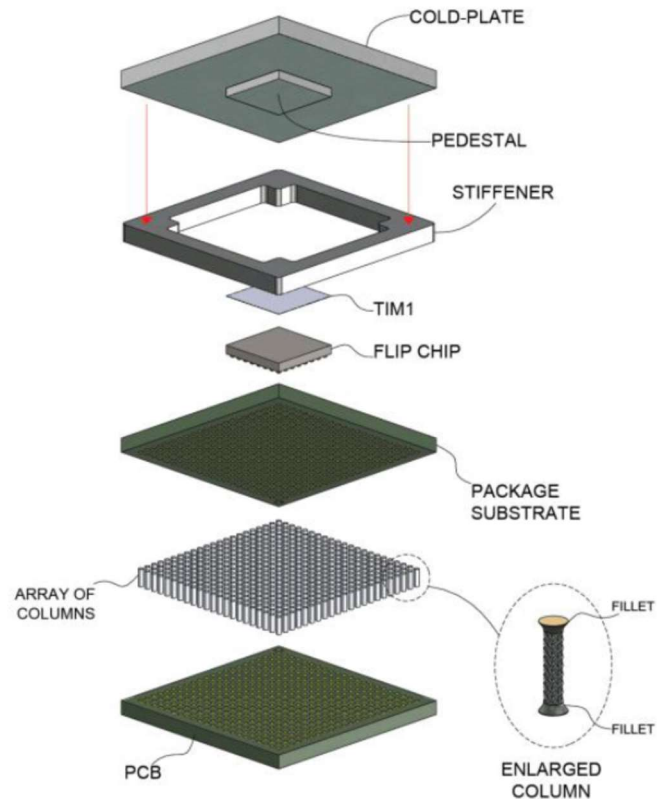


Figure 7. Exploded view of AI package connecting to PCB with copper-core columns instead of solder balls.

The paper characterizes the mechanical and thermal properties of individual columns and examines how column geometry influences tensile strength, compliance, and calculated thermal conductance. Data tables show that columns exhibit higher modeled thermal-conductance values than solder balls, supporting modeled watt-level heat transport per column and illustrating how array-level conductance can scale with pin count in both terrestrial and space-oriented design scenarios. These results are presented at the column level. Package-level performance and reliability outcomes for fully assembled arrays depend on the complete system design and are outside the scope of the data reported here.

Although composite columns carry a higher per-unit fabrication cost than solder balls, their combination of mechanical compliance and conductive cross-section makes them candidates for applications where thermal transport and interconnect mechanics are critical design constraints. Potential implications for cooling overhead, system-level power consumption, or total cost of ownership depend on specific package and data-center architectures and require application-specific validation or reference to prior work. In this context, the column data presented here are intended to inform design tradeoffs rather than to establish system-level economic or reliability advantages.

This study also provides practical design guidance, including pad-to-column diameter ratios, stencil geometries, solder-coating selection, and column-length considerations. These guidelines support the engineering evaluation of column-based interconnects as a possible replacement for solder balls on existing substrates, with the aim of addressing fatigue and strain mechanisms associated with CTE mismatch, warpage, and thermal cycling. Copper-core columns are discussed as a structural and thermal-transport option for cryogenic systems, aerospace platforms, AI accelerators, HPC servers, co-packaged optics (CPO) modules, switch ASICs, and emerging glass-core substrate architectures, where conventional solder balls may face increasing limitations as semiconductor packaging evolves toward larger substrates, higher power densities, and more demanding operating conditions. Future work and referenced literature can extend these column-level findings to validated package-and system-level reliability and performance assessments.

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