

Copper Core Columns for AI Data Centers

Brief

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ABSTRACT

AI data centers are entering a period of unprecedented thermal and mechanical stress. Rack power is rising from 132 kW and is rapidly heading toward 600 kW. Chip package sizes are expanding beyond historical limits, and immersion cooling is introducing sporadic thermal transients that conventional solder-ball interconnects cannot survive. These converging forces create a physics-of-failure environment that demands a new class of interconnect.

Copper-core columns provide a tunable thermal and mechanical structure capable of surviving next-generation loads. This paper presents the physics basis for column adoption. We discuss the architectural advantages of TopLine's patented and patent pending column technology, the reliability methodology, and the forecasted market expansion that supports a global licensing ecosystem.

INTRODUCTION

AI workloads are driving a rapid escalation in data-center thermal density. As GPU packages grow in size and power, the interconnect requirement (historically an afterthought) has become a critical reliability bottleneck. Traditional solder balls were never designed for the thermal flux, mechanical strain, and immersion-cooling dynamics now emerging in modern AI systems.

AI chip package sizes already exceed 70mm and are rapidly moving beyond 180 mm and approaching 300 mm footprints. These geometries introduce significant warpage, higher CTE mismatch, and greater cold-plate pressure. At the same time, immersion cooling is becoming mainstream, creating aggressive ΔT transients that solder balls cannot absorb.

The industry is approaching a solder-ball failure cliff. Columns provide the first viable path forward.

THE PHYSICS PROBLEM

Three independent failure modes are converging in AI data centers:

1. Thermal Escalation

Rack power is rising sharply. Even with advanced cold-plates, localized hotspots and transient thermal spikes propagate through the package stack. Solder balls lack the thermal mass and conductivity to dissipate these loads. The rack gets even hotter with the trend towards increasing rack voltage systems from 48V to 800V.

2. Mechanical Strain and Warpage

Large AI packages introduce significant mechanical deformation. Warpage during reflow and operations generate shear forces that exceed the mechanical limits of solder balls. The introduction of glass-core substrates promises to reduce warpage. Unfortunately, glass-core technology introduces even more strain caused by severe coefficient-of-thermal-expansion (CTE) mismatch. Solder balls can not survive such extreme stresses.

3. Immersion-Cooling Transients

To cool down powerful heat generating chip packages, a new technology known as immersion cooling has a side-effect of introducing rapid temperature swings and fluid-driven shock loads. ΔT is scientific notation that means "change in temperature". These ΔT transients create cyclic stresses that solder balls cannot withstand.

Individually, each failure mode is challenging. Together, they create a reliability environment that exceeds the physics limits of solder-ball interconnects.

WHY SOLDER BALLS FAIL

Solder balls fail because their geometry and material properties are fundamentally mismatched to next-generation AI packages. Five categories of solder ball failure are explained below.

1. Insufficient Ball Height

Solder balls are short spherical structures. Their limited height concentrates strain at the interface, increasing the likelihood of cracking under warpage and thermal cycling.

2. Limited Mechanical Compliance

Solder balls cannot flex enough to absorb CTE mismatch between large packages the PCB. As package size increases, strain rises exponentially causing solder ball failures to accelerate.

3. Low Buckling Stability

Cold-plates are utilized to cool down chip packages. However, solder balls have a tendency to collapse or deform, when combined with immersion-cooling and thermal shock loads, compromising electrical and thermal integrity under the clamping pressure of cold-plates.

4. Poor Thermal Pathways

Solder balls do not provide a meaningful thermal path to the PCB. As package power increases, they become thermal bottlenecks.

5. Transient Vulnerability

Rapid temperature swings (ΔT) in immersion cooling environments create cyclic fatigue that solder balls cannot survive.

The physics-of-failure is clear: solder balls are no longer viable for next-generation AI packages.

COLUMN ARCHITECTURE OVERVIEW

Copper-core columns are engineered to address the thermal, mechanical, and reliability challenges of modern AI systems. Column designs are tunable by intentionally selecting its geometry and material characteristics in order to adjust performance across chip package zones (regions). Column tunability facilitates optimized package performance.

Copper Core

A high-strength copper core provides superior thermal conductivity and mechanical stability. It

acts as a heat path from the package to both the cold-plate and the PCB.

Meshed Sleeve

A compliant copper meshed sleeve surrounds the copper core, enabling controlled mechanical flexibility. This sleeve absorbs strain and distributes load across the column height.

Solder Selection

The braided sleeve is covered by a choice of malleable solder coatings that encapsulates the column and mechanically binds the sleeve to the core.

RELIABILITY METHODOLOGY

TopLine's reliability methodology is designed to validate column performance under the full spectrum of AI data-center stresses. These testing methodologies ensure columns meet or exceed reliability thresholds required by GPU vendors, OSATs, and hyperscalers.

Destructive Bend Testing

Bend testing measures column compliance and mechanical robustness of different materials under extreme deformation.

Pull-Strength Testing

This testing validates column attachment integrity at the pads and core-sleeve bonding strength.

Thermal Cycle Testing

This widely recognized form of reliability testing.

ΔT Transient Testing

This testing simulates immersion-cooling shock loads and rapid ΔT events.

Warpage and Strain Mapping

Finite Element Analysis (FEA) is used to model strain distribution across large packages and glass-core substrates.

TAM – MARKET EXPANSION FORECAST

The transition from solder-ball interconnects to copper-core columns are driven by structural changes in AI data-center architecture. As rack power increases and chip package footprints expand, the number of interconnects per rack grows

proportionally. This creates a steep upward trajectory in total available market (TAM).

By 2030, TAM for column interconnects is projected to reach \$18 billion, driven by:

- Larger AI package footprints
- Increased rack density
- Adoption of immersion cooling
- Higher interconnect counts per chip package

By 2035, TAM is expected to exceed \$30 billion, with annual column demand surpassing 600 billion units. This growth reflects both the scaling of AI infrastructure and the physics-driven necessity of column adoption.

Columns are more than a niche improvement over solder-balls. Columns are a foundational shift in interconnect technology.

SOM – SHARE OF MARKET ADOPTION MODEL

The initial Share of Market (SOM) is conservatively estimated at 5% by 2030, based on early adoption by GPU vendors and OSATs. This baseline reflects a realistic ramp aligned with reliability validation and equipment readiness.

SOM opportunity: Market-pull demand is anticipated to increase sharply once reliability data is validated.

After columns are qualified and standardized, the SOM could accelerate significantly. Further, if columns become adopted as the preferred interconnect class across multiple GPU families, then SOM could rise toward 25%, creating a multi-billion-dollar licensing opportunity.

This adoption model is supported by:

- Physics-of-failure limits of solder balls
- Package size growth beyond 140 × 180 mm
- Immersion-cooling transients
- Glass-core substrate expansion
- Hyperscaler demand for improved uptime and lower total cost of ownership (TCO)

ECONOMIC IMPACT OF COLUMNS

Columns provide a dual-path heat-transfer mechanism:

- Upward conduction into the cold-plate
- Downward conduction into the PCB

This dual-path transfer of heat reduces localized hotspots and improves thermal uniformity across the package.

Lower Electricity Consumption

By improving thermal efficiency, columns reduce the cooling energy required to maintain rack stability. This directly lowers electricity consumption at Hyperscaler scale.

Lower Total Cost of Ownership (TCO)

Columns reduce TCO by:

- lowering cooling energy costs
- improving package reliability
- reducing downtime caused by solder-ball failures
- enabling larger, more powerful AI packages

For Hyperscalers, even small improvements in thermal efficiency translate into significant operational savings.

STAKEHOLDER ADOPTION DYNAMICS

Column adoption follows a predictable sequence across the semiconductor ecosystem.

GPU Vendors

GPU vendors are expected to be the first movers. As package sizes increase and thermal loads rise, columns become essential for reliability and performance.

OSAT (Outsourced Semiconductor Assembly and Test)

It is anticipated that OSATs will adopt columns only after GPU vendors qualify them. OSATs benefit from improved yield, reduced rework, and more predictable reliability.

Hyperscalers

There is a reasonable likelihood that Hyperscalers may accelerate adoption after solder-ball failures

begin impacting data center uptime. Columns reduce TCO and improve operational stability, making them attractive for large-scale deployments.

SUPPLY CHAIN ECOSYSTEM

The copper-core column ecosystem spans multiple layers of the semiconductor supply chain. Each participant plays a distinct role in ensuring reliable, scalable deployment across AI data-center infrastructure.

Column Manufacturer

Column makers, such as TopLine, produce copper-core columns at scale. Responsibilities include braiding a meshed wire sleeve over a copper-alloy core, solder coating, inspection, cutting, deburring, and final packing. Column makers supply OSATs, substrate manufacturers, and advanced packaging facilities.

OSATs

OSATs attach columns to package substrates and interposers. Their workflows include column loading, solder paste dispensing, column transfer, reflow (soldering) attachment, planarizing, cleaning, and inspection. OSATs are the critical link between column manufacturers and GPU vendors.

GPU Vendors

Typically, GPU vendors do not manufacture columns nor attach columns. Instead, GPU vendors qualify column technology through OSATs and substrate partners. Their adoption decisions drive ecosystem alignment.

EMS Providers

Electronics Manufacturing Services (EMS) companies are responsible for printed circuit board assembly (PCBA) of chip packages (with columns previously attached by OSATs) together with other electro-mechanical and electronic components. EMS vendors also provide box-build and rack-assembly for hand-off to Hyperscalers. EMS can influence GPU vendor, OSAT adoption and Hyperscaler decision making.

Hyperscalers

Hyperscalers design the rack architecture, set exact hardware and thermal specifications and outsource manufacturing and box builds to Original Design Manufacturers (ODM) and EMS providers.

Hyperscalers consume column-enabled packages indirectly. Operational requirements, such as uptime, thermal efficiency, and TCO influence GPU vendor and OSAT adoption. This multi-tier ecosystem ensures that column technology scales globally without requiring GPU vendors or Hyperscalers to modify their existing supply-chain roles.

LICENSING FRAMEWORK (RAND)

TopLine's roadmap includes a licensing model structured to support global scalability while maintaining fairness and predictability across all partners. The framework follows RAND principles (Reasonable and Non-Discriminatory) ensuring consistent terms for all licensees.

EARLY ADOPTION PROGRAM

TopLine will offer a limited number of early-adopter licenses to strategic partners capable of scaling rapidly and contributing to ecosystem development.

Benefits for Early Licensees

Early licensees demonstrate market-readiness and gain a competitive edge as column adoption accelerates.

- Access to reliability data during the beta-test phase
- Participation in tuning refinement
- Influence over ecosystem standards and best practices
- First-mover advantage prior to JEDEC standardization
- Strategic positioning with GPU vendors and hyperscalers

EXPANSION INTO NEW MARKETS

Copper-core columns unlock new opportunities beyond terrestrial AI data centers. Their thermal efficiency, mechanical compliance, and reliability under extreme conditions make them suitable for emerging markets. Below are examples of emerging markets known at the time of this writing. Additional market areas for columns are expected to be discovered. These markets expand the long-term TAM and create additional licensing opportunities for partners.

Space-Based Data Centers

Copper-core columns exhibit performance behaviors that provide reliable performance under radiation, vacuum, and thermal cycling, capable of supporting future space-based compute infrastructure.

Cryogenic Systems

Some varieties of copper-core and solder-core columns maintain structural integrity at cryogenic temperatures, enabling applications in quantum computing and low-temperature electronics.

High-Performance Embedded Systems

Columns enable larger, more powerful embedded packages where solder-ball reliability is insufficient.

Aerospace and Defense

Some varieties of copper-core and solder-core braided columns withstand vibration, shock, and thermal extremes, making them suitable for aerospace and defense systems requiring high-reliability interconnects in a tin-lead solder environment.

Glass-Core Substrates

Glass-core substrates are anticipated to reduce warpage; however, such technology introduces even more strain caused by severe coefficient-of-thermal-expansion (CTE) mismatch between glass-core chip substrates and the PCB where solder-ball reliability is insufficient.

Lunar Surface Exploration

A race to deploy encampments and roving vehicles on regions of the Lunar surface where extreme temperature swings (ΔT) make solder-ball reliability impractical. Copper-core columns provide thermal transport and mechanical stress relief suitable to Lunar surface missions.

STRATEGIC IMPLICATIONS

The transition to column interconnects represents a once-in-a-generation shift in semiconductor packaging. As AI workloads intensify and package sizes grow, columns will become the defining interconnect class for high-power systems.

This shift creates strategic opportunities for:

- Column manufacturers
- OSATs
- Substrate makers

- Materials suppliers
- Equipment vendors
- Hyperscalers seeking lower TCO

Partners who adopt column technology early will be positioned to lead the next era of AI infrastructure.

ONCE-in-a-GENERATION OPPORTUNITY

The semiconductor industry rarely encounters a shift driven so directly by physics. As AI packages expand and thermal loads intensify, the interconnect layer becomes a limiting factor in system reliability and performance. Solder-ball technology, which has served the industry for decades, is now constrained by geometry, material properties, and thermal behavior that cannot scale to meet next-generation demands.

Copper-core columns represent a structural solution to this physics-of-failure problem. Their tunable thermal and mechanical characteristics allow them to operate reliably across large package footprints, immersion-cooling environments, and high-power workloads. These capabilities position columns potentially as the defining interconnect class for the next era of AI infrastructure.

The transition to columns is not optional. It is inevitable. Partners who engage early will shape the standards, influence ecosystem alignment, and secure long-term strategic advantage.

WHY TOPLINE LEADS

TopLine is uniquely positioned to lead the global transition to column-based interconnects. TopLine's leadership is rooted in physics, IP, and market alignment, not marketing claims.

Several factors contribute to this leadership:

Foundational IP Portfolio

TopLine holds a robust portfolio of granted and pending patents covering core metallurgy, braided sleeve construction, column geometry, compliance physics, thermal pathways, and manufacturing methods. This IP foundation provides long-term defensibility and ecosystem stability.

First-Mover Advantage

TopLine is the first to develop tunable column architecture with optimization rules across zoning (regions) of chip packaging and interposer

structures. This early innovation positions TopLine as the reference model for column design and reliability.

Prototype Manufacturing Capability

TopLine maintains in-house capability to produce prototype columns and samples as well as Daisy Chain test vehicles. This accelerates reliability testing, partner evaluation, and GPU vendor qualification.

Market Tailwinds

Industry trends, including larger packages, immersion cooling, higher power voltage regulator modules (VRM) from 48V to 800V, glass-core substrates, and Hyperscaler total-cost-of-ownership (TCO) requirements, align directly with column advantages. TopLine's technology is positioned at the intersection of these forces.

Early Customer Interest

Engagement from GPU vendors, OSATs, substrate makers, and materials suppliers demonstrates strong market readiness and validates the need for a scalable licensing ecosystem.

STRATEGIC PARTNER ENGAGEMENT

TopLine is actively engaging strategic partners capable of scaling copper-core column technology across global supply chains.

These partners include:

- Column manufacturers
- OSATs
- Substrate makers
- Materials suppliers
- Equipment vendors
- Advanced packaging innovators

COLUMN ARCHITECTURE DIAGRAMS

This portfolio covers core metallurgy, braided mesh sleeve construction, column geometry, compliance physics, thermal pathways, and manufacturing methods. It forms the foundation of TopLine's licensing ecosystem and ensures long-term IP superiority.

TopLine's patent portfolio (As of Nov 2026) includes:

- US 10,477,698 B1
- US 10,937,752 B1
- US 12,526,920 B1
- US 9,629,269 B1
- US 9,108,262 B1
- CN 11822899 B
- CN 114055006 B

Additional patents are pending.

TopLine welcomes confidential technology licensing discussions and access to proprietary reliability IP for qualified partners and early interest adopters.

Confidential Licensing Inquiry Contact:

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